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COMPUTER ASSISTED DESIGN OF CURRENT MODE OP-AMP

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COMPUTER ASSISTED DESIGN OF CURRENT MODE OP-AMP

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This work is dedicated to my family

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Acknowledgements

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Abstract

Objectives of this thesis work, is mainly to design a high current gain using 0.5μm CMOS technology and Low-voltage class AB current amplifiers. Also, it will be a clue for other engineers to design on the current mode op amp in further modification. A high-gain current-mode operational amplifier has been studied which is current-mode counterpart of traditional voltage-mode operational amplifier. Low voltage current mode circuits are essential for the mobile communication devices and portable electronic systems because low voltage reduces the problem related to power dissipation and reliability issues, while the current mode design techniques offer voltage independent high bandwidth analog circuits which are useful in high frequency circuit design applications. Voltage mode circuits that were used in the past can now be implemented using current conveyors. Also along with the use of current mode circuits (CMCs) it is desired to have simple design as they are expected to give better results due to less complexity and so there is effort for circuits that employ simple topologies. The use of current mode circuits will gain more and more importance as the development in portable electronics will advance.

The application of class-A current amplifiers is limited by the small current swing because a large current swing would require the quiescent point to be far away from the pinch-off, resulting in a large drain-source voltage. To accommodate high-current applications, class AB configurations that employ a pair of NMOS and PMOS current mirrors activated separately are effective.

The simulation results in the study like, the open loop gain is improved by more than four fold and the power dissipation of the device is reduced highly by 97% from the specification. These results specially mets the objectives or the target of the thesis.

Chapter 1

Introduction

1.1 The operational amplifier

Operational amplifiers (op-amps) are widely used in signal processing circuits, control circuits, and instrumentation circuits. Of all analog integrated circuits, the op-amp is the analog integrated circuit which has the most sales and is the most widely used in a variety of electronic circuits. It's an important component for electrical engineers who design circuits using it and to all other kinds of engineers who use measurement and control circuits that contain operational amplifiers [1,2]. The operational amplifier is a versatile component that can do many things in measurement, signal processing and control. That versatility is the main reason that one finds so many operational amplifiers being used. Operational amplifiers are used in many places including:

- In strain gage circuitry to measure deformations in structures like bridges, airplane wings and I-beams in buildings.
- In temperature measurement circuitry for boilers and in high altitude aircrafts in a cold environment.
- In control circuits for aircraft, people movers in airports, subways and in many different production operations.

In electronics, small signal amplifiers are commonly used devices as they have the ability to amplify a relatively small input signal, for example from a sensor such as a photo-device, into a much larger output signal to drive a relay, lamp or loudspeaker.

Table 1.1: Classification of Amplifiers

Based on size of Signal	Based on Physical Configuration (for BJTs)	Based on duration (angle) of output signal	frequency of operation
Small Signal	Common Emitter	Class A Amplifier	Direct Current (DC)
Large Signal	Common Base	Class B Amplifier	Audio Frequencies (AF)
	Common Collector	Class AB Amplifier	Radio Frequencies (RF)
		Class C Amplifier	VHF,UHF and SHF

There are many forms of electronic circuits classed as amplifiers, from operational amplifiers and small signal amplifiers up to large signal and power amplifiers. Not all amplifiers are the same and are therefore classified according to their circuit configurations and methods of operation. The classification of an amplifier depends upon the size of the signal, large or small, its physical configuration and how it processes the input signal, that is, the relationship between input signal and current flowing in the load [3,4]. Table 1.1: gives the classification of amplifiers based on such characteristics.

An amplifier can be thought of as a simple block containing the amplifying devices with two input terminals and two output terminals (ground being common) where the output signal is much greater than that of the input signal due to amplification [5]. Generally, an ideal signal amplifier has three main characteristics: infinite input resistance ($R_{in} = \infty$), zero output resistance ($R_{out} = 0$) and infinite open loop gain or ($A = \infty$). No matter how complicated an amplifier circuit is, a general amplifier model as shown in figure 1.1 can be used to show the relationship of these three properties.

1.2 Ideal Amplifier Model

Amplifier Gain:

Amplifier gain is simply the ratio of the output divided by the input. The ratio of the output voltage to the input voltage is known as the voltage gain of the amplifier and is basically a measure of how much an amplifier amplifies the input signal [5,6]. Gain has no units as it is a ratio, and it is commonly given the symbol A, for amplification.

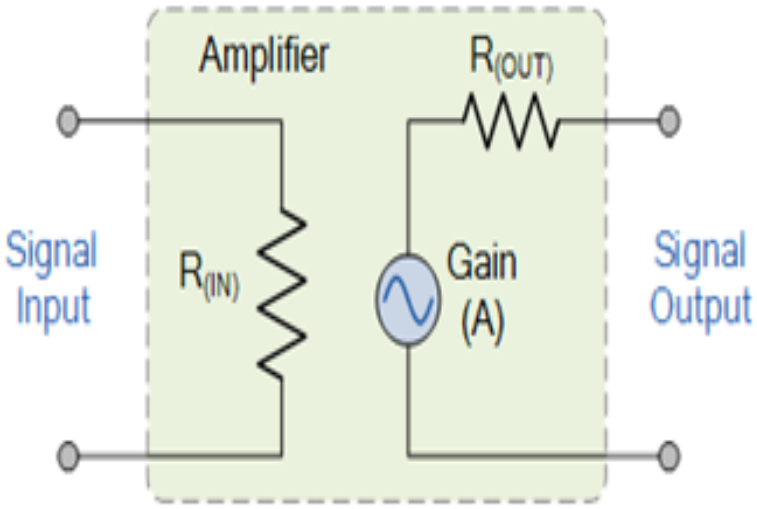

Figure 1.1: Ideal Amplifier Model

We can classify amplifier gain into three: Voltage Gain (A_V), Current Gain (A_I) and Power Gain (A_P) depending upon the quantity being measured, as shown in figure 1.2.

When calculating the gain of an amplifier, the subscripts V, I and P are used to denote the type of signal gain being measured, that is voltage, current, or power, respectively. Mathematically they are expressed as:

$$Voltage\ gain\ (A_v) = \frac{out\ put\ voltage}{input\ voltage} = \frac{V_{out}}{V_{in}} \tag{1.2.1}$$

$$current\ gain\ (A_i) = \frac{out\ put\ current}{input\ current} = \frac{I_{out}}{I_{in}} \tag{1.2.2}$$

$$power\ gain\ (A_p) = \frac{out\ put\ power}{input\ power} = \frac{P_{out}}{P_{in}} \tag{1.2.3}$$

Over the last a few years, the electronics industry has exploded in terms of research and design. Operational amplifiers are key elements in analog processing systems integral part of many analog and mixed signal systems. As the demand for mixed mode

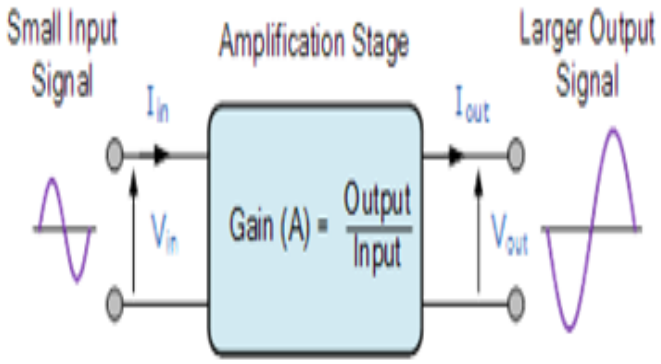

Figure 1.2: Amplifier Gain of the Input Signal

integrated circuits increases, the design of analog circuits such as operational amplifiers (op-amps) in complementary metal-oxide semiconductor (CMOS) technology becomes more critical [7]. In CMOS op-amp technology, we have two circuit modes, namely: voltage mode and current-mode circuits. Compared to the voltage-mode counterparts, current mode circuits are preferred especially for their wider bandwidth, lower power consumption and larger dynamic range [7, 8]. Current-mode operational amplifier (COA) is one of the most important devices and it is the exact current-mode counterpart of the traditional voltage-mode amplifier (VOA). It means that almost all VOA-RC analog circuits can be alternatively implemented as COA-RC ones by using adjoint network principle [9]. COA ideally exhibits zero input resistance and infinite output resistance and current gain.

1.3 Development of integration technologies

Integrated Circuit (IC) also referred to as a monolithic integrated circuit is an assembly of different electronic components connected together electronically on one small semiconductor wafer (usually silicon). An IC is also called as a chip or a microchip. An integrated circuit is defined as a circuit in which all or some of the circuit elements are inseparably associated and electrically interconnected so that it is considered to be indivisible for the purposes of construction and commerce.

Today's ICs have millions or even billions of electronic components like transistors, resistors, diodes, flip-flops, Multiplexer (MUX), Demultiplexer(DEMUX), etc., integrated (interconnected) together on a single unit which is very small in size, usually equivalent to the size of a fingernail. All the electronic equipment today use a number of Integrated circuits. ICs have revolutionized the world of electronics. After the invention of ICs all electronic components like mobile phones, computers and other home appliances have become cheaper and smaller in size. Integrated Circuits can perform a number of operations such as amplification, oscillators, memory storage, arithmetic and logical operations etc [10].

The need for integrated circuit

The operations today performed by ICs were earlier performed by using either vacuum tubes or discrete semiconductor devices. Vacuum tubes consisted of electrodes inside a vacuum glass tube. They were slower in operation, expensive and bigger in size. In order to make technical advancements it was necessary to increase the number of these components which in turn would increase the cost and size. Also, previously all the components were individually connected whereas today different components in an IC are printed as a single unit using photolithography. Very thin paths of metal like copper and aluminum are laid directly on the same piece of material. These thin paths function like wires and electrically integrate all the different components of the integrated circuit [11].

History of integrated circuits

In 1958 Jack Kilby, an engineer of Texas instruments, successfully demonstrated the first working integrated circuit device. The first customer to this new invention was the US Air Force. In the year 2000 Jack Kilby won the Nobel Prize in Physics for miniaturized electronic circuits.
One and a half years after Kilby demonstrated his IC design, Robert Noyce of Fairchild Semiconductor Limited came up with his own integrated circuit. His model solved many practical problems which Kilbys device had. It was made up of silicon where as Kilbys was made up of germanium. Jack Kilby and Robert Noyce both received US patents for their part of work on integrated circuits. The earlier developed ICs had only few transistors and resistors on the chip [7].

In the early 1960s, Small Scale Integration (SSI) circuits were manufactured. SSI circuits consisted of few tens of components on a single chip. Philips TAA320 is an example of SSI design. By the late 1960s Medium Scale Integration (MSI) devices came into existence which had hundreds of transistors on a single chip. MSI devices were less expensive and allowed more complex systems in very less space. Further development in the mid 70s led to Large Scale Integration (LSI) devices which had thousands of transistors per chip. An example of a LSI device is 1KB RAM. In early 80s Very Large Scale Integration (VLSI) was introduced. Today we have very complex devices such as Ultra Large Scale Integration (ULSI), System On Chip (SOC), Wafer Scale Integration (WSI) and Three Dimensional Integrated Circuits (3D-IC).

There are two broad classes of ICs. These are digital and analog. Digital ICs work only on two defined levels 1s and 0s. They can contain millions of logic gates, flip-flops etc integrated on a single chip. Microprocessors and microcontrollers are examples of digital ICs. Analog ICs work by processing continuous signals. Sensors and op-amps are examples of analog ICs. They perform functions such as filtering, amplification, modulation, demodulation etc. Sometimes analog and digital ICs can be combined on a single chip. Such ICs are called as mixed signal or hybrid integrated circuits [12].

The development of modern integration technologies is normally driven by the needs of digital CMOS circuit design. As the sizes of integrated devices decrease, where maximum voltage ratings also rapidly decrease. Thus, if we want to utilize the fastest integration technologies currently available, we are usually restricted to active components in the design of integrated analog circuits. Since the introduction of integrated circuits, the op-amp has served as the basic building block in analog circuit design. Since then, new integrated analog circuit applications have emerged and the performance requirements for analog circuits have changed. Voltage-mode operational amplifier circuits have limited bandwidth at high closed-loop gains due to the constant gain-bandwidth product [13].

Furthermore, the limited slew-rate of the op-amp affects the large-signal, high-frequency operation. When wide bandwidth, low power consumption and low voltage operation are needed simultaneously. The voltage-mode operational amplifier easily

becomes too complex and has characteristics that are not needed, for example DC-accuracy. On the other hand, circuit techniques used in radio frequency applications are usually too simple to reach the required accuracy. Therefore, there is a growing need for new, low voltage analog circuit techniques.

CMOS is a technology used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors, data converters and highly integrated transceivers for many types of communication. Frank Wanlass patented CMOS in 1963 [1].

CMOS is also sometimes referred to as complementary-symmetry metal-oxide semiconductor (or COS-MOS) [7]. The word "complementary-symmetry" refers to the fact that, the typical digital design style uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions [8].

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair of MOSFETs is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic devices, for example transistor-transistor logic (TTL) or n-type metal oxide semiconductor (NMOS) logic, which normally has some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips.

The recent progress of analog technology has bred several modern active devices, i. e the monolithic IC active components and functional blocks. They are versatile and powerful building blocks for many signal processing systems.

1.4 The current mode

Originally, the term current-mode processing was coined by Barrie Gilbert when he worked on strict trans-linear loops [7], in which the voltages truly are incidental. Nowadays we are persuaded that current-mode integrators, filters, and oscillators

have some special merit. In contrast to strict trans-linear loops, current-mode circuits rely on an intimate dialogue between voltage signals and current signals. When comparing current-mode to voltage-mode circuits, it is most important to focus on their operations than the difference in their definitions [14].

The current-mode approach is mainly an alternative way of looking at analog IC design, and not a tool to classify circuits. Taken in this sense, the current-mode idea is a powerful concept mainly because it broadens the horizon of analog IC design. The difference in the performances between voltage-mode and current-mode circuits is that voltage-mode and current-mode circuits are often built with different design techniques. Voltage-mode circuits often use higher loop gains than current-mode circuits, and current-mode circuits are often made less complex than the voltage-mode circuits they are compared to, simply by the designers preferences [15].

The traditional op-amp and the transimpedance op-amp (also known as current feedback op-amp) are unquestionably two of the most flexible and widely used analog integrated circuits of today. However, as the standard supply voltages for digital circuitry are decreasing significantly, so are the signal ranges for the analog components (especially in mixed analog- and digital-mode systems). An attempt to overcome this problem can be simply to change the signal representation from a voltage to a current. In this way the signal range is no longer directly restricted by the supply voltage but also dependent on the impedance level chosen by the designer.

In the process of designing current-mode circuits, it can be advantageous to follow the ″Theory of Adjoint Networks″ [7, 8]. This theory is a conversion strategy which, when applied to a given voltage-mode circuit, leads to a current-mode circuit with the same transfer function. This thesis describes an attempt to obtain a useful structure for a current-mode op-amp by applying the ″Theory of Adjoint Networks″ to the traditional op-amp and to the transimpedance op-amp on a subcircuit level. Most current amplifiers described in the open literature have only limited gain [9, 16]. However, the structure described in this research study is suitable for true COA operations, i.e. a current gain in the order of $>$ 2dB.

1.4.1 current conveyors-history and presence

Current conveyors were considered to be used as controlled voltage and current sources, impedance converters and inverters, etc., but also as function generators, amplifiers, filters, etc., in current processing circuits, mainly for instrumentation and measurement applications [9]. In the first years of their appearance, the performance of current conveyors was severly limited by the available technologies, which did not allow well-matched devices on fabricated chips [16]. Since the technologies have improved in the eighties, the current conveyors gained the attention of many analog designers. Today the current conveyors have developed to very useful building blocks of analog electronics. They are parts of a number of very often used circuits, like active filters, transimpedance and 'current feedback' operational amplifiers, voltage and current operational amplifiers etc., and their main application areas are in high-speed, high-frequency circuits for both voltage and current signal processing. The current conveyor approach to the design of current operational amplifiers was the first attempt to design high-current-gain amplifiers [14,17].

One of the most basic building blocks in the area of current-mode analogue signal processing is the current conveyor (CC). It is a four (in basic form) terminal device which when arranged with other electronic elements in specific circuitry can perform many useful analogue signal processing functions. In many ways, current conveyor simplifies circuit design in much the same manner as the conventional operational amplifier. The current conveyor offers an alternative way of abstracting complex circuit functions, thus aiding in the creation of new and useful implementations. Moreover, CC is a mixed-mode universal building block (in VLSI terms), which can substitute classical op-amps in voltage-mode applications or gives us a chance to transform these applications to current-mode.

Many papers have demonstrated the universality, advantages and novel applications of the current conveyor since its first introduction in 1968 [8, 14]. Concurrently with these papers, a number of authors have outlined improved implementations designed to enhance the performance and utility of this circuit building block. Unfortunately, there is still lack of available current conveyors in the form of IC. Due to this fact, many designers cannot use this block in their developed applications and systems. If the situation changes, the designers will get the chance to be more familiar

with the current conveyor and its usability. There is only one monolithic IC of pure current conveyor: CCII01. Paradoxically, many novel constructions of modern wide band and high-speed op-amps are based on current conveyor (OPA660, AD840) [17].

1.4.2 Evolution of current-mode building blocks

The current-conveyor represents the first building block intended for current signal processing. The enhanced version of the current-conveyor: the second-generation current-conveyor (CCII) appeared in 1970 [18]. Neither of these building blocks became popular as a consequence of the introduction of the integrated op-amp at the time. As the voltage-mode op-amp concept had already been introduced in the 1940s, it is no wonder that the current-conveyor did not become a success overnight. Additionally, integrated current-conveyors were difficult to realize due to the lack of high performance pnp-devices in the integration technologies of the 1970s.

In the 1980s, fast vertical pnp-devices were introduced in bipolar integration technologies. During that time, research groups started to notice that the voltage-mode op-amp is not necessarily the best solution to all analog circuit design problems. New research findings regarding current-mode signal processing using current-conveyors were presented. Furthermore, a commercial product, that is, the current-feedback op-amp became available [7, 19]. The high slew rate and wide bandwidth of this amplifier resulted in its popularity in video amplifier applications.

The current-feedback op-amps rely on the complementary bipolar process technology. In order to realize current-mode circuits with the less expensive CMOS-technology, different circuit topologies and operation principles are required. In 1988, the principle of a MOS current copier was presented which enabled sampled data circuits using only MOS-transistors [20, 10]. In 1989 the switched-current (SI) principle was presented [21]. The SI-circuits represent an alternative to the switched-capacitor (SC) circuits that do not need linear capacitors. SI-circuits can therefore be realized with a standard digital CMOS-process.

Several improvements to this circuit technique have been presented, for example

the second generation SI-integrator [10] and the SI2-technique [14] to reduce current memory errors with a two-step sampling method. Following the introduction of sampled-data signal processing using current-mirrors, continuous-time filter realizations based on current-mirrors were also reported [22, 23, 24]. Furthermore, various proposals for a CMOS current-mode operational amplifier have been published, either with a differential input and single-ended output [25] or with a single-ended input and differential output [26].

1.5 Background and Motivation for current mode circuit design

One procedure for finding alternative, preferably simpler, circuit realizations is to use current signals rather than voltage signals for signal processing [7, 8]. MOS transistors in particular are more suitable for processing currents rather than voltages because the output signal is current both in common-source and common-gate amplifier configurations and common-drain amplifier configurations and are almost useless at low supply voltages because of the bulk effect present in typical CMOS-processes. Moreover, MOS current-mirrors are more accurate and less sensitive to process variations than bipolar current-mirrors because with the latter the base currents limit the accuracy. Therefore, at the very least, MOS transistor circuits should be simplified by using current signals in preference to voltage signals. For this reason, integrated current-mode system realizations are closer to the transistor level than the conventional voltage-mode realizations and therefore simpler circuits and systems should result [10].

When signals are widely distributed as voltages, the parasitic capacitances are charged and discharged with the full voltage swing, which limits the speed and increases the power consumption of voltage-mode circuits. Current-mode circuits cannot avoid nodes with high voltage swing either but these are usually local nodes with less parasitic capacitances. Therefore, it is possible to reach higher speed and lower dynamic power consumption with current-mode circuit techniques. Current-mode interconnection circuits in particular show promising performance [9, 10]. When the signal is conveyed as a current, the voltages in MOS transistor circuits are proportional to the square-root of the signal, if saturation region operation is assumed for

the devices. Similarly, in bipolar transistor circuits, the voltages are proportional to the logarithm of the signal. Therefore, a compression of voltage signal swing and a reduction of supply voltage are possible. This feature is utilized for example in log-domain filters [16], switched current filters [21], and in non-linear current-mode circuits in general.

Unfortunately, as a consequence of the device mismatches, this non-linear operation may generate an excessive amount of distortion for applications with high linearity requirements. Thus, in certain current-mode circuits, linearization techniques are utilized to reduce the nonlinearity of the transistor transconductance, in which case the voltage signal swing is not reduced. However, the compression of the voltage signal swing, for example, increases sensitivity to mismatches. Similarly, a large amount of reported current-mode circuits require advanced complementary bipolar integration processes utilizing vertical npn- and pnp-transistors with a high f_T, circuits which need excessively high supply voltages in order to be useful in most battery operated applications.

Furthermore, some current-mode techniques such as the current-feedback are very old (compared to cathode-feedback in electron tube amplifiers) and are used as enhanced voltage-mode signal processing building blocks rather than as true current-mode signal processing building blocks. At radio frequencies, current-mode circuit techniques are limited to on-chip signal processing in integrated circuits as off-chip impedance levels are fixed, typically at 50. However, the aggressive scaling of integration technologies ensures that current-mode circuit techniques will remain useful in the future, while some longer on-chip sub-system interconnections may need RF design techniques.

The current-mode design technique is a good alternative for the high performance analog circuit design as it offers voltage independent high bandwidth. In current-mode design, the stress is more on the current levels for the operation of the circuits and the voltage level at various nodes are immaterial. In Voltage-mode circuits (VMCs), such as operational amplifiers (op amps), the performance of the circuit is determined in terms of voltage levels at various nodes including the input and the output nodes. But all these circuits suffer from the following disadvantages:

- Output voltage cannot change instantly when there is a sudden change in the

input voltage due to stray and other circuit capacitances.

- Bandwidth of the op amp based circuits is usually low because of finite unity gain bandwidth.
- Slew rate is dependent on the time constants associated with the circuit.
- Circuits do not have high voltage swings.
- Require higher supply voltages for better signal-to-noise ratio.

Therefore, VMCs are not suitable for high frequency applications.

An ideal voltage-mode circuit has infinite input impedance, zero output impedance and a constant voltage gain. The best example of voltage mode circuit is an ideal operational amplifier. The infinite input impedance and a zero output impedance of Operational amplifiers enable an easy cascade without loading effect and also ensure that the characteristics of these circuits are determined by the external elements [21].

Unlike ideal voltage-mode circuits, an ideal current-mode circuit has the characteristics of zero input impedance, infinite output impedance and a constant current gain. The current amplification will result in a high level of static power consumption; therefore, the current gain of ideal current-mode circuits is set to unity. This constant current gain up to large frequency range enables current-mode circuits to be used for high frequency applications. On the contrary, the gain of voltage-mode circuits falls at high frequencies [1].

1.5.1 Common-Mode Linearized Amplifiers

Increasing the linear input range of the input stage optimizes op-amp large signal distortion. This can be accomplished through the use of architectures such as degenerated differential structures and class AB input stages, both of which increase noise and lower precision. An alternate method is to linearize using a common-mode structure whose noise is rejected by the inherent differential nature of the input stage while also maintaining such precision metrics as common mode rejection ratio (CMRR), power supply rejection ratio (PSRR), and offset voltage (VOS). Analog devices have numerous new amplifiers that now feature the common-mode linearized input architecture [3].

1.5.2 Differential Amplifiers

Differential amplifiers allow the process of single-ended input to complementary differential outputs or differential inputs to differential outputs. These amplifiers feature two separate feedback loops to control the differential and common-mode output voltages. The differential amplifiers of analog devices are configured with a VOCM pin, which can be easily adjusted for setting output common-mode voltage. This provides a convenient solution when interfacing with analog-to-digital converters (ADCs) [1]. In this thesis, a CMOS current operational amplifier (COA) with fully differential input and differential output designed and implemented from a differential current mirror input transimpedance stage followed by a differential output transconductance gain stage was studied. This configuration is the current-mode counterpart of the traditional voltage operational amplifier (VOA) [20, 26].

1.6 Adjoint principle

As a wide range of voltage-mode analogue circuits already exist, a straight forward method of converting these voltage-mode circuits to current-mode circuits would be very useful. In such a method, a circuit using voltage amplifiers and passive components converted into one that contains current amplifiers and passive components. Direct replacement of a voltage amplifier with a current amplifier will lead to different circuit behavior [10].

A voltage-mode circuit can be converted into a current-mode circuit by constructing an interreciprocal network by using the adjoint principle [7, 18, 10]. According to this principle, a network N is replaced with an adjoint network Na, where the voltage excitation is interchanged to a current response and the voltage response is interchanged to a current excitation, as shown in figure 1.3.

Thus, the resulting transfer functions of these two networks N and Na are identical:

$$H_v(S) = \frac{V_{out}}{V_{in}} = \frac{i_{out}}{i_{in}} = H_i(S) \tag{1.6.1}$$

When the networks N and Na are identical, for example in the case of passive networks, the networks are said to be reciprocal to one another. Since all passive networks

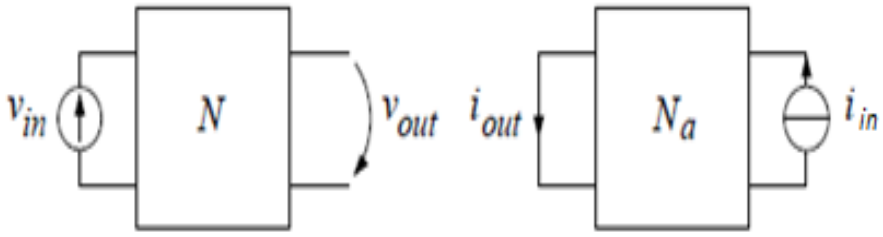

Figure 1.3: Adjoint principle network (Interreciprocal networks N and Na).

are reciprocal, all passive circuit elements have themselves as their adjoint elements, i.e., passive elements are inter-reciprocal. In order to maintain identical transfer functions for both the original network N and the adjoint network Na, the impedance levels in the corresponding nodes of both networks should be identical. Therefore, the signal flow is reversed in the adjoint network and a voltage source is converted to a current sensing element as they both behave as short circuits. Similarly, a voltage sensing element is converted to a current source [27]. A list of circuit elements and their adjoint elements are presented in figure (1.4).

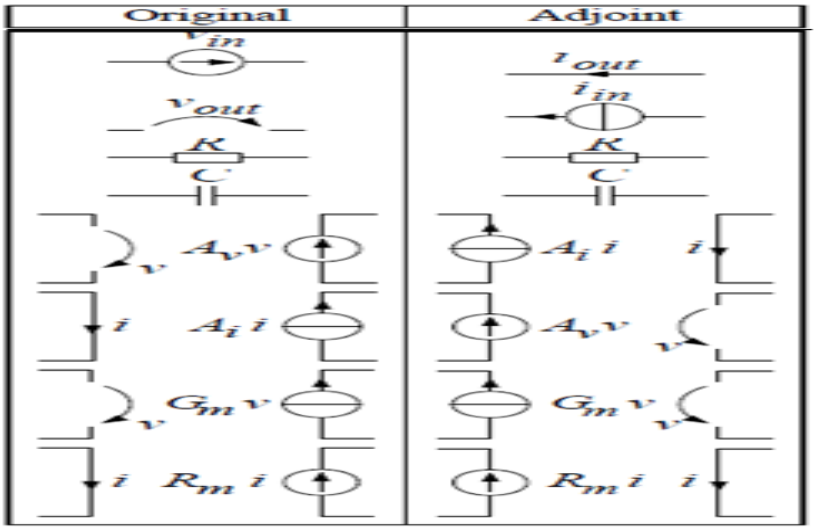

Figure 1.4: Some circuit elements with their corresponding adjoint elements

In addition, controlled sources can be converted with the same principle: the signal flow is reversed and the impedance level is kept the same. In this way, a voltage amplifier is converted to a current amplifier and a current amplifier is converted to a voltage amplifier, respectively. However, since transresistance and transconductance amplifiers are inter-reciprocal, networks containing only transresistance or transconductance amplifiers and passive elements differ only in signal direction and type.

The adjoint principle can also be applied to transistor level circuits. In this case, a bipolar transistor in a common-emitter amplifier configuration is inter-reciprocal to itself and the common-collector amplifier configuration has the common-base configuration as its adjoint. Converting a voltage-mode bipolar transistor circuit to a current-mode MOS transistor circuit could be beneficial as it minimizes the use of source-follower stages which have poor low-voltage performance due to the bulk effect. Bipolar transistor circuits are conventionally constructed of common-emitter and common-collector amplifier stages and the resulting MOS transistor adjoint circuit is constructed from common-source and common-gate amplifier stages.

Organization of the thesis work

The thesis is organized as follows:

CHAPTER 1: INTRODUCTION. This chapter gives an idea on the need for an op-amp, its classification, model and gain. The development of integrated technologies, VLSI and CMOS were introduced. Finally, the definition, evolution, background and motivation for the current mode circuits and the adjoint principle were given.

CHAPTER 2: LITERATURE SURVEY. This chapter covers the past and present researches on the current-mode and voltage mode circuits with respect to input and output impedance, slew rate, power supply rejection ratio, bandwidth, propagation delay and electrostatic discharge etc. It also covers various current-mode circuit design techniques.

CHAPTER 3: MATHEMATICAL FORMULATIONS OF THE CURRENT MODE OP-AMP. This chapter discusses the circuit layout, specification, and the mathematical formulations of the current mode op-amp.

CHAPTER 4: RESULTS, CONCLUSION AND SCOPE FOR FUTURE WORK. Analysis of graphical results have been done in this chapter. Conclusions drawn from the results are given. Also, possible suggestions and scope for future improvements have been discussed.

Chapter 2

Review of Literature

Needs of low-voltage design of analog integrated circuits have been increasing recently [7]. Down-scaling into sub-microns in advanced VLSI fabrication technologies demands lowering of supply voltages for digital circuits [7]. This also demands analog circuits to be operable with low supply voltages since analog signal processing circuits are usually implemented in the form of an analog-digital mixed system on a VLSI. On the other hand, development of portable telephone systems also drives analog circuits to be operable with low supply voltages since portable telephones are powered by dry batteries [8]. In order to establish low-voltage analog circuit techniques compatible with CMOS technologies, several approaches have been tried: the application of back-gate control in a MOS translinear circuit [9], the use of subthreshold operation of MOSFETs [16], etc.

A current-mode CMOS circuit is a promising solution to low-voltage analog CMOS circuit design since it is theoretically operable with a supply voltage of several hundreds millivolts greater than the threshold voltage of a MOSFET [21]. In current mode CMOS circuits, the addition of the signals has been possible only in current mode so that the addition and subtraction of signals are power consuming operations and the circuit design flexibility have been limited by its nonlinear I-V and V-I conversions.

A floating gate MOSFET (FG-MOSFET) enables linear addition of signals in voltage mode and it is implementable using a standard double-poly CMOS technology [1, 20]. The addition of signals by an FG-MOSFET does not consume DC power since the addition is performed by capacitive coupling [1]. The threshold voltage is

linearly controllable by the gate voltage whereas the threshold control through the back-gate results in nonlinear dependence [1]. Even a depletion type MOSFET is realizable from an enhancement-type MOSFET by applying an appropriate gate-bias voltage to the gate of the FG-MOSFET. This property is useful for realizing low-voltage analog circuit building blocks [19].

In addition, when the above functions of FG-MOSFETs are combined with a current-mode CMOS circuit technology, a circuit designer can enjoy both its enhanced design flexibility and its suitability to low-voltage CMOS circuit design.

2.1 Voltage Mode to Current Mode

Compared to voltage-mode circuits, current-mode ones have such advantages as high slew rate, high bandwidth, simple circuitry and low voltage operation [7, 8]. Due to the small voltage swings associated with the low-impedance nodes, current-mode circuits can operate with low power supply voltages. Low voltage operation of current mode circuits has gained more importance due to today's semiconductor technology scaling down trend and reliability issues. This trend of technology has led to the popularity of mixed-mode System-on-Chips (SOCs) in which analog and digital circuits are integrated on one chip. Thus, along with low voltage operation, analog designers have to concern about power supplies and ground fluctuations caused by the switching of the digital portion of mixed analog-digital circuits. Hence, low voltage structures with Power Supply Rejection Ratio (PSRR) and common mode rejection ratio (CMRR) so high to suppress those noticed noises as well as other unwanted common mode signals are critically needed. Fully differential signal processing is commonly used in many fields mainly because of its inherent immunity to common mode signals, clock feed through, interferences and other types of common mode disturbances [9, 27,28].

One procedure for finding alternative, preferably simpler, circuit realizations is to use current signals rather than voltage signals for signal processing. MOS-transistors in particular are more suitable for processing currents rather than a voltage because the output signal is current both in common-source and common-gate amplifier configurations and common-drain amplifier configuration is almost useless at low supply voltages because of the bulk-effect present in typical CMOS-processes. Moreover, MOS current-mirrors are more accurate and less sensitive to process variation than

bipolar current-mirrors because with the latter the base currents limit the accuracy.

Therefore, at the very least, MOS-transistor circuits should be simplified by using current signals in preference to voltage signals. For this reason, integrated current-mode system realizations are closer to the transistor level than the conventional voltage-mode realizations and therefore simpler circuits and systems should result.

There are several good reasons why current mode signals should be considered. Although errors can be introduced into any signal, voltage mode signals are susceptible to more than their share of problems [28].

- These include the impedance of the voltage source and other supply fluctuations, wire and connection resistance, the integrity of wire insulation, electrostatic and electromagnetic noise, and ground potential differences. Care must be taken not to load a voltage signal as new devices are added.
- The only real advantage of voltage mode signals is that they interface directly with D/A and A/D converters and analog multiplexing devices.
- Current mode signals are immune to loop resistance found in long wire runs and faulty connections. Additional devices generally can be added to the loop without concern for the signal, supply permitting.
- Current mode signals are relatively immune to noise, the only exception being electromagnetically induced noise which can be substantially eliminated through the proper use of shielded twisted pairs.

Thus, we can now explain why current-mode circuits are considered to be faster than voltage-mode circuits: although both would be similarly good from an ideal point of view, over-peaking caused by second-order effects makes problems close to the GBW product of the feedback op-amps. It is important to see that, the same over peaking effects also occur in CCIIs that use local feedback to reduce the input resistance of the X terminal; in this case, the speed advantage of the CCII vanishes. Furthermore, one can also build open-loop voltage amplifiers that show no over peaking.

However, it turns out that, circuits without local stabilizing feedback are just more typical for the current-mode approach. Both the transfer function of the closed-loop

op-amp and the behaviour of the CCII are determined by the low-impedance nodes of the circuits only. These low-impedance nodes all look similar in both voltage-mode and current-mode circuits: a transistor gm sets the node resistance, parasitic capacitances of transistors set the node capacitance, and the voltage swing is limited by transistors that would otherwise leave the region of saturation. Thus, the non-dominant poles and zeros will be at similar frequencies, and the harmonic distortion at high frequencies and the noise properties will also be similar.

What mainly determines the performance of a circuit is the number of low-impedance nodes and the way they are connected, i.e., the complexity of a circuit determines the performance of an amplifier or filter. As with feedback, one finds that less complex circuits are more typical for the current-mode approach, but there are a few voltage-mode circuits with reduced complexity, like the very fast G_mC filters presented in [10]. They were built with operational transconductance amplifiers (OTAs) that only have input and output nodes, but no internal nodes at all. Of course, current-mode circuits can also be made more complex to improve their linearity and signal-to-noise ratio, but that slows them down again. Thus, the advantages of current-mode circuits that are often cited in the literature, like a potential for reaching higher frequencies, lower power consumption, and smaller chip area, are in fact real, but the reason is not technical, and has nothing to do with choosing voltages or currents to represent signals. The reasons for the difference are mainly the design preferences of the proponents of the current-mode approach [9].

2.1.1 Current and Voltage Source Comparison

Most sources of electrical energy (mainly electricity, a battery, ...) are best modeled as voltage sources. Such sources provide constant voltage, which means that, as long as the amount of current drawn from the source is within the source's capabilities, its output voltage stays constant. An ideal voltage source provides no energy when it is loaded by an open circuit (i.e. an infinite impedance), but approaches infinite power and current when the load resistance approaches zero (a short circuit). Such a theoretical device would have a zero ohm output impedance in series with the source. A real-world voltage source has a very low, but non-zero output impedance: often much less than 1 ohm.

Conversely, a current source provides a constant current, as long as the load connected to the source terminals has sufficiently low impedance. An ideal current source would provide no energy to a short circuit and approach infinite energy and voltage as the load resistance approaches infinity (an open circuit). An ideal current source has an infinite output impedance in parallel with the source. A real-world current source has a very high, but finite output impedance. In the case of transistor current sources, impedances of a few megohms (at DC) are typical. An ideal current source cannot be connected to an ideal open circuit because this would create the paradox of running a constant, non-zero current (from the current source) through an element with a defined zero current (the open circuit).

Also, a current source should not be connected to another current source if their currents differ but this arrangement is frequently used (e.g., in amplifying stages with dynamic load, CMOS circuits, etc.) Similarly, an ideal voltage source cannot be connected to an ideal short circuit (R=0), since this would result a similar paradox of finite nonzero voltage across an element with defined zero voltage (the short circuit). Also, a voltage source should not be connected to another voltage source if their voltages differ but again this arrangement is frequently used (e.g., in common base and differential amplifying stages).

On the contrary, current and voltage sources can be connected to each other without any problem and this technique is widely used in circuitry (e.g., in cascode circuits, differential amplifier stages with common emitter current source, etc.) Because no ideal sources of either variety exist (all real-world examples have finite and non-zero source impedance), any current source can be considered as a voltage source with the same source impedance and vice versa. These concepts are dealt with by Norton's and Thvenin's theorems.

2.2 Voltage Processing Circuits versus Current Processing Circuits

The increasing popularity of digital designs and the respective tailoring of the technologies for digital signal processing requires new design techniques for analog circuits, which are considered to be fabricated on a common chip with digital functions [9, 16].

The scaling down of the dimensions of the devices is also accompanied by a respective scaling of supply voltages [21], what sets directly an upper limit for the dynamic range of the signal, if this is processed as voltage. The result of such a development is that special rail-to-rail building blocks for voltage signal processing have to be designed and used [1, 18, 19].

An alternative for solving the above described problems offer current processing circuits. Here, the decreasing of the supply voltage does not directly limit the dynamic range of the signal processing circuits. In addition, the immunity of current processing circuits to the digital noise, which can be found on supply voltage rails of mixed analog and digital circuits, expressed by the means of power supply rejection ratio having the dimension of ohms, is better to control in current processing circuits [20]. A very interesting feature of current processing circuits is also their ability to be used in high- performance voltage processing applications. Recently voltage amplifiers based on current controlled current sources, which achieve much higher frequency parameters than conventional voltage operational amplifiers [10, 14]. Obviously, taking the adjoint network theorem into account, voltage controlled voltage sources can be used in high-performance current processing applications too.

2.2.1 Analog Signal Processing

The growing integration of electronics technology allowed digital circuits to become superior to the conventional analog circuits for signal processing. This is because the digital signal is defined only in discrete values of time and amplitude, typically in a binary weighted sum of signals having only two defined values of amplitude. On the contrary, the analog signal is defined in a continuous range of time and amplitude, what makes it much more sensitive to interferences due to technology variations and noise. In addition, digital circuits offer a better possibility to memorize the processed signal, the signal processing can be changed by software inside a solidly designed hardware, and last but not least, the simulation of digital signal processing can be done on block or system level without requiring sophisticated models for active devices [7, 29].

Taking these advantages of digital circuits into account, the designers are forced to look for digital solutions rather than analog in VLSI systems. Therefore much more effort has been devoted to the development of circuits, technologies and design tools

for digital rather than analog signal processing. Nevertheless, there are two reasons, why analog signal processing will be always required in some form. Practically, all signals in the physical world are continuous in both amplitude and time, and hence always analog techniques will be required for conditioning of such signals before they can be processed in digital signal processing circuits [18, 30].

The second important reason for the requirement of analog signal processing is the bandwidth, which can be some order of magnitudes higher, if the signal is processed in analog circuits than in digital.
The superiority of digital signal processing is also expressed by the technologies for the fabrication of the chips, which are tailored mainly for digital signal processing. The classical analog bipolar technology is abdicating to the favour of the much cheaper and for digital signal processing more suitable CMOS technology.

To be able to keep the high performance of analog signal processing circuits also on digital technologies the designers have to look for new principles for the design of circuits for analog signal processing. Terms like switched capacitors, current mode and switched currents are appearing more and more in diverse scientific and technical journals and educational publications. The current signal processing as a part of analog signal processing is gaining an increasing attention of analog designers because of its supplemental properties to the more classical voltage signal processing and it offers also some advantages over the old, continuous-time, voltage-mode design techniques.

2.3 Current and Voltage Conveyors

Classical voltage operational amplifier (VOA) is one of the most famous and commonly used blocks. VOA can be described as active building block that operates in voltage-mode. Another similar block is voltage follower (VF). A number of blocks with reciprocal behavior to previous voltage mode blocks have been proposed during the last 15 years. Current operational amplifier (COA) and current follower (CF) can be mentioned as examples. Moreover, some of the basic building blocks can operate in both, voltage and current modes. This type of block has been termed as mixed-mode. Mixed-mode block usually has both, "voltage" and "current" terminals. The most famous mixed-mode active block is current conveyor [8, 9]. Nowadays, current

conveyors appear in many modern constructions of wideband and high-speed operational amplifiers, etc [17].

2.3.1 Current Conveyors

The current-conveyor is intended as a general building block as with the operational amplifier. Because the operational amplifier concept has been active since the late 1940s, it was difficult to get any other similar widely accepted concepts. However, operational amplifiers do not perform well in applications where a current output signal is needed and consequently there is an application field for current-conveyor circuits. Since current-conveyors operate without any global feedback, a different high frequency behavior compared to operational amplifier circuits results [18, 20].

Analog VLSI can address almost all real world problems and finds exciting new information processing applications in a variety of areas such as integrated sensors, image processing, speech recognition, hand writing recognition etc [29]. All conventional analog circuits viz., op-amps, voltage to frequency converters, voltage comparators etc. are voltage mode circuits, which suffer from low bandwidths arising due to the stray and circuit capacitances and are not suitable in high frequency applications. The need for low-voltage low-power circuits is immense in portable electronic equipment like laptop computers, pace makers, cell phones, etc. Voltage mode circuits are rarely used in low-voltage circuits as the minimum bias voltages depend on the threshold voltages of the MOSFETs. However, in current mode circuits, the currents decide the circuit operation and enable the design of the systems that can operate over wide dynamic range. The low end of the circuit operating range is limited by the leakage currents and noise floor level while the high end is decided by degradation of the transconductance per unit current available above the threshold voltage [7].

These circuits can give large bandwidths and are suitable for low-voltage applications. Current feedback amplifiers, operational floating conveyors, current conveyors (CCs) etc. are the popular current mode circuit structures. The most widely used structure among them is the CCII structure [8]. In this work we present some of the emerging applications of the CCs and the classification schemes.

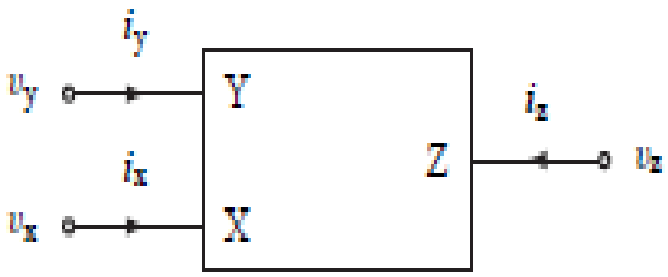

Figure 2.1: Symbol used for all types of current conveyors [8].

A CC is a three or more port (X, Y, and Z) network. Port X is a hybrid port and functions as input port for current signals and output port for voltage signals at the same time. Port Y is a voltage input port and port Z is a current output port, which can either sink or source current equal to the current injected into port X. If port Y is connected to a potential V, an equal voltage will appear on the port X and if a current I is forced through port X, an equal current will flow through port Y (depending upon the nature of the CC, see fig.2.2). The same current I, the sign of which is governed by the current transfer characteristics as shown in fig. 2.2, is also conveyed and supplied through output port Z at a high impedance level in the manner of a current source and so the output current remains unaffected by the load. The potential at port X is independent of the current I forced into X and the current I through port Y is independent of the voltage V applied to Y. Thus, the device exhibits a virtual short circuit input characteristic at port X and a dual virtual open-circuit input characteristic at port Y [8, 9, 18].

The current conveyors have been classified in three classes viz, CCI, CCII, and CCIII. All the three have similar structures but their characteristics are different. Current conveyors are commercially available (e.g., AD 844 from Analog Devices) [7].

The commonly used block representation of a CC is shown in figure 2.1, whose input-output relationship is given by,

$$i_y = 0 \times v_y + A \times i_x + 0 \times v_z = A \times i_x \tag{2.3.1}$$

$$v_x = B \times v_y + R_X \times i_x + 0 \times v_z = B \times v_y + R_X \times i_x \tag{2.3.2}$$

$$i_z = 0 \times v_y + C \times i_x + 0 \times v_z = C \times i_x \tag{2.3.3}$$

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & A & 0 \\ B & R_X & 0 \\ 0 & C & 0 \end{bmatrix} \cdot \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix}$$

Figure 2.2: Matrix or current conveyors equation [2].

where i_x (v_x), i_y (v_y) ,and i_z (v_z) are the currents (voltages) at ports X, Y, and Z respectively. C characterizes their current transfer from X to Z and A is related to the nature of the conveyor. That is A, B, C assume a value either 1, 0 or ± 1 and R_X is the intrinsic resistance offered by the port X to the input currents.

For an ideal CC, $V_X = V_Y$ and the input resistance (R_X) at port X is zero (fig.2.2 matrix equation). But in practical CCs, R_X is a nonzero positive value. So the equivalent symbol of a CC should include R_X in its representation and the popular CC symbol is shown in figure 2.1 [9]. The equivalent circuits are used to analyze the complex circuits. One can understand that, the circuit operation is better when the complex structures are simplified using equivalent circuits.

2.3.2 Classification of Current Conveyors

There are several schemes for classification of CCs. Most common techniques among them are based on the characteristics of its ports X, Y and Z [31]. CCs have also been classified similar to power amplifiers based on the quiescent current flow.

2.3.3 Port Y Based Classification

Port Y is used as input for voltage signals and it should not load the input voltage source by drawing current. But in some applications, it is desirable to draw currents from the input voltage source.
When port Y draws a current equal to the current injected at port X, $A = 1$, according to the matrix equation in figure2.2. This configuration is termed as first generation current conveyor.
When port Y draws zero current ($A = 0$), it is second generation current conveyor.
Similarly, when this current equals to the current injected at port X but of opposite polarity, the configuration is known as third generation current conveyor for which A = -1 [8, 9, 18].

- $C > 0$, the circuit is a positive transfer conveyor (CC+)
- $C < 0$, the circuit is a negative transfer conveyor(CC-).
- $A = 1$, the circuit is a first generation current conveyor (CCI)
- $A = 0$, the circuit is a second generation current conveyor (CCII)
- $A = -1$, the circuit is a third generation current conveyor (CCIII)

It is desired that, a CC should have large bandwidth and consume low quiescent power.
Ideally a CC should have,

- Infinite input impedance (R_{in}) at port Y
- Zero input impedance (R_x) at port X for current inputs
- Infinite output impedance (R_{out}) at port Z
- Unity voltage transfer gains between port Y and X
- Unity current transfer gain between port X and Z
- Infinite bandwidth

2.3.4 First Generation Current Conveyors (CCI)

The network of the first generation current-conveyor CCI has been formulated in a matrix form as follows in fig. (2.3) [7]:
where the + sign applies for positive current conveyors denoted as CCI+, in which

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix}$$

Figure 2.3: Matrix of the first generation current-conveyor CCI.

the current flows into both the X- and Z-terminal in the same direction and the - sign stands for the opposite polarity of the X-to-Z-terminal current transfer of the negative current conveyor CCI-.
The first generation current conveyor (CCI) forces both the currents and the voltages in ports X and Y to be equal and a replica of the currents is mirrored (or conveyed) to the output port Z [8].

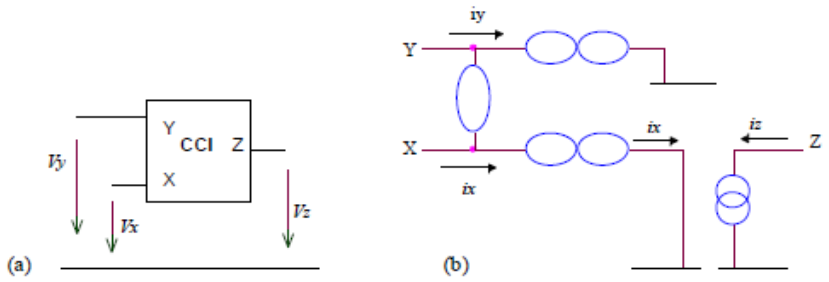

Figure 2.4: The first generation current conveyor: a) symbol and b) its signal definition,Nullator.

2.3.5 Second Generation Current Conveyor CCII

For many applications, a high impedance input terminal is preferable and to increase the versatility of the current conveyor, which no current flows in terminal Y. For these reasons, the second generation current-conveyor was developed. It has one high and one low impedance input rather than the two low impedance inputs of the CCI [8, 32]. This building block has been proven to be more useful than CCI. CCII can be described by following the matrix when the current flowing into CCII+ or out of

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix}$$

Figure 2.5: Matrix of Second Generation Current Conveyor CCII.

CCII-, the Z node is proportional to the current flowing into the X node.

The second-generation current-conveyor is a principle of voltage-follower with a voltage input Y node and a voltage output X node, and a current-follower (or current inverter) with a current input X and a current output Z connected together [8].
CCII has proven to be by far more useful of the current conveyor family types. Wide

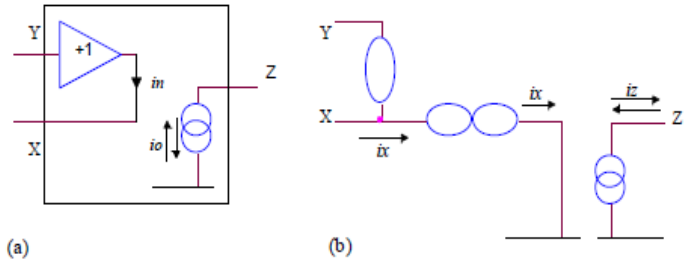

Figure 2.6: a) The principle of the second generation current conveyor:CCII+,iz=ix. CCII-,-iz=ix. b) Nullator-norator CCII complete scheme.

range of applications was published. It is very suitable building block for design of the active-RC filters or number of special admittance converters. In the last decade the numbers of high-speed and wide-range op-amps are based on current conveyor structure. Also for low voltage applications CCII is starting to be very powerful building block.

2.3.6 Third Generation Current Conveyor CCIII

Yet another current-conveyor was proposed in 1995 [8, 9, 24]. The network of this third generation current-conveyor CCIII is formulated in a matrix form as shown in figure (2.7). This type is similar to CCI, there is opposite current transfer between X and Y terminal. The input current flows into the Y-terminal and out from the X-terminal, one might think that a differential current input could be realized with this amplifier. However, the CCIII has high input impedance with common-mode current signals, i.e. identical currents are fed both to Y- and X-terminals. Therefore common-mode currents can push the input terminals out from the proper operation range. This current-conveyor can be used as an active current probe.

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix}$$

Figure 2.7: Third Generation Current Conveyor CCIII matrix.

2.3.7 Port X Based Classification

For voltage signals, port Y serves as input port and now port X serves as output port. The output voltage at port X can either have same polarity as that of the input voltage (V_Y) ; in this case current conveyor is called as non-inverting CC, or that of opposite polarity ; are termed as inverting CCs [19].
The inverting second generation current conveyor positive (ICCII+), has the following port relation between terminal voltages and currents:

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix}$$

Figure 2.8: Port relation between terminal voltages and currents for inverting second generation current conveyor-positive (ICCII+).

2.3.8 Port Z Based Classification

Port Z is the current output port and usually, the magnitude of the output current at port Z equals to the magnitude of the current injected into port X. In some cases,

however, this amplitude may be scaled version (generally up scaled) of the input current and also the direction of the current may be same or opposite to that of the current in port X. CC with positive current output is termed as CC+ and with negative output currents as CC- [10, 14].

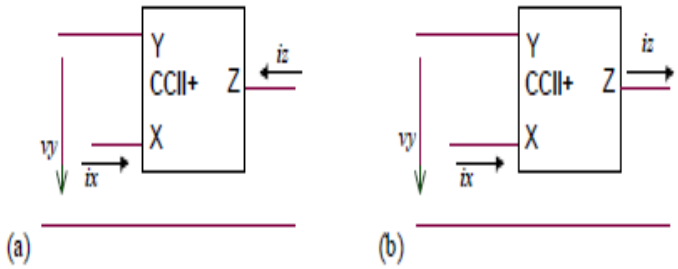

Figure 2.9: (a) Negative CCII, (b) Positive CCII basic blocks.

A CC can have two or more output ports, which can independently sink or source currents. Such a CC is known as multi port CC. A multi port CC with both types of output ports (positive as well as negative), is known as composite port CCII.

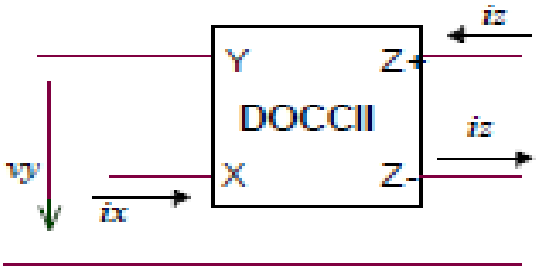

Figure 2.10: Dual output CCII basic blocks.

2.3.9 CCII Applications

Because of the separate voltage and current inputs, both voltage and current amplifiers can easily be realized with the second-generation current conveyors and the

gain can be set by resistor ratios as in operational amplifier circuits. Signal processing in current conveyor circuits is based on voltage-to-current and current-to-voltage conversions and on signal buffering by voltage and current buffers. Since there is typically no feedback in current conveyor circuits, wide bandwidth operation without any slewing at large signal amplitudes is achieved. The conventional applications of CCs include amplifiers, oscillators, filters, wave shaping circuits, analog computers etc... [14, 25]. Low-voltage and low-power architectures of CCs are particularly suitable in the design of voltage and power starved systems.

2.4 characteristics of current mode circuits

In this section, comparison between voltage mode and current mode circuits with respect to input/output impedance, bandwidth, slew rate, propagation delay, power supply sensitivity etc. have been discussed.

2.4.1 Input and Output Impedances

It was pointed out earlier that, a voltage mode circuits is featured by large input impedance and low output impedance. On the contrary, a current-mode circuit possesses low input impedance and high output impedance [22].

$$
\begin{aligned}
i_o &= i_{o1} + i_{o2} \\
v_{o1} = v_{o2} \Longrightarrow i_{o1} z_o &= i_{o2} z_{in} \\
\Longrightarrow \frac{i_{o1} z_o}{i_{o2} z_{in}} &= 1 \\
= \frac{i_{o1}}{i_{o2}} &= \frac{z_{in}}{z_o} \\
= \frac{i_o - i_{o2}}{i_{o2}} &= \frac{z_{in}}{z_o} \\
= \frac{i_o}{i_{o2}} - 1 &= \frac{z_{in}}{z_o} \\
= \frac{i_o}{i_{o2}} &= 1 + \frac{z_{in}}{z_o} \\
= \frac{i_{o2}}{i_o} &= \frac{1}{1 + \frac{z_{in}}{z_o}} \\
i_{o2} &= \frac{1}{1 + \frac{z_{in}}{z_o}} i_o
\end{aligned}
$$

The loading current is given by

$$
i_{o2} = \frac{1}{1 + \frac{z_{in}}{z_o}} i_o \approx \left(1 - \frac{z_{in}}{z_o}\right) i_o \tag{2.4.1}
$$

where z_o and z_{in} are the output impedance of the driving stage and the input impedance of the driven stage respectively. Note that $z_{in} << z_o$ was assumed and rationalizing the denominator is also applied in simplifying equation 2.4.1. To minimize the loading effect, $z_{in} << z_o$ is required for current mode circuits. Similarly, when the input is represented by its Thevenin equivalent, the loading effect of the voltage mode circuits can be studied and the load voltage is given by,

$$
v_{o2} = \frac{1}{1 + \frac{z_{in}}{z_o}} v_o \approx \left(1 - \frac{z_{in}}{z_o}\right) v_o \tag{2.4.2}
$$

To minimize the loading effect, $z_{in} >> z_o$ is required for voltage-mode circuits [1]

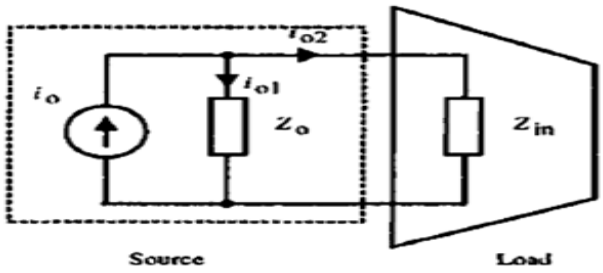

Figure 2.11: The loading effect in current mode circuits.

2.4.2 Bandwidth

The bandwidth of voltage mode and current mode circuits can be best compared using the building blocks of voltage/current mode circuits shown in figure (2.12) and 2.13).

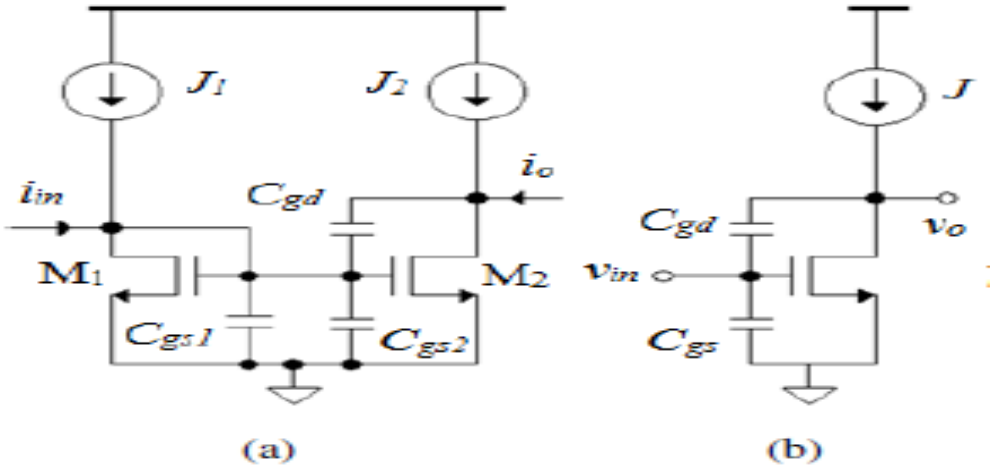

Figure 2.12: Bandwidth comparison of voltage-mode and current-mode circuits (a) Basic current mirror; (b) Common-source amplifier..

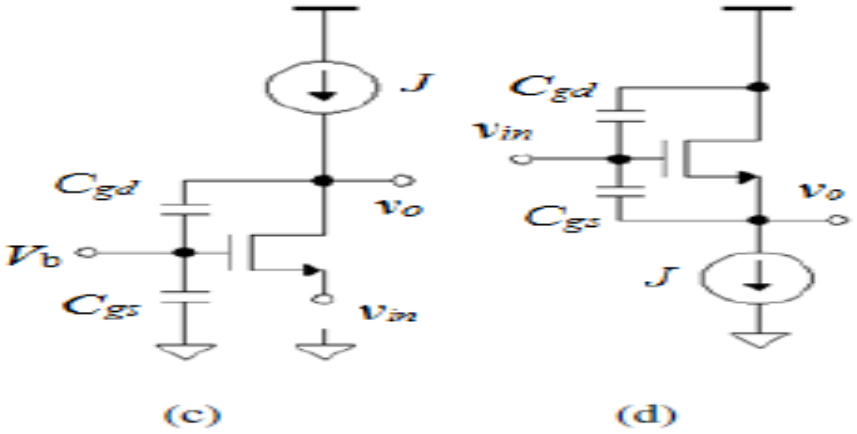

Figure 2.13: Bandwidth comparison of voltage-mode and current-mode circuits (c) Common-gate amplifier; (d) Source follower..

Since a well designed current mode cirrcuit has large output impedance and small input impedance, the load impedance $z_L \approx 0$ holds. As a result M_2 of the basic current mirrior is not subject to Miller effect. The only pole of the basic current mirror is at the gate of M_{1-2} with the pole frequency given by,

$$\omega_p \approx \frac{g_{m1}}{C_{gs1} + C_{gs2} + C_{gd2}} \tag{2.4.3}$$

Due to the existence of the floating gate-drain capacitor C_{gd}, the common-source configuration is subject to Miller effect with Miller capacitances $C_{m1} = C_{gd}(1 + g_m r_o)$ at the gate and $C_{m2} = C_{gd}\left(1 + \frac{1}{g_m r_o}\right)$ at the drain, where r_o and g_m are the output impedance and transcondutance of the transistor, respectively. The pole at the input called Miller pole, is given by,

$$\omega_{in} = \frac{1}{R_s\left(C_{gs} + C_{gd}(1 + g_m r_o)\right)} \tag{2.4.4}$$

where R_s is the resistance of the source. The output pole is estimated from

$$\omega_o \approx \frac{1}{r_o\left(C_{gd} + C_{in}\right)} \tag{2.4.5}$$

where C_{in} is the input capacitance of the load stage.

The common gate configuration is not subject to Miller effect due to the absence of floating capacitors. The pole at the input is given by,

$$\omega_{in} \approx \frac{1}{R_s C_{gs}} \tag{2.4.6}$$

and the pole at the output is computed from,

$$\omega_o \approx \frac{1}{r_o \left(C_{gd} + C_{in}\right)} \tag{2.4.7}$$

The source follower is also free of Miller effect simply because its small signal voltage gain is approximately unity. The Miller capacitances at the gate and source are given by $C_{m1} \approx C_{m2} \approx 0$. The pole at the input is also given by equation (2.4.6)and the dominant pole at the output is given by,

$$\omega_o \approx \frac{1}{r_o C_{in}} \tag{2.4.8}$$

For practical applications, C_{in} and r_o are often large; the dominant pole of the common-source common-gate and source follower amplifiers are usually at the output node. The pole frequency of the basic current mirror is therefore smaller as compared to the pole frequency of the basic voltage-mode amplifier [1].

2.4.3 Slew Rate

Slew Rate can be measured by checking the steepest rise of a square wave response. It is commonly used in electronics to check the rise time between 10% and 90%. The slew rate of an operational amplifier may be important in many applications. The op-amp slew rate is particularly an important parameter in applications where the output is required to switch from one level to another quickly. In these applications the rate at which the op-amp can change between the two levels is important. The slew rate of an op-amp or any amplifier circuit is the maximum rate of change in the output voltage caused by a step change on the input. It is measured as a voltage change in a given time - typically: $\frac{V}{S}$ or V/μs.

A typical general purpose device may have a slew rate of 10V/μs. This means that, when a large step change is placed on the input, the device would be able to provide an output 10 volt change in one microsecond. The figures for slew rate change are dependent upon the type of operational amplifier being used. Low power op-amps

may only have figures of a volt per microsecond, whereas there are fast operational amplifiers capable of providing rates of $1000\text{V}/\mu s$.

Op-amps may have different slew rates for positive and negative going transitions because of the circuit configuration. They have a complementary output to pull the signal up and down. This means, the two sides of the circuit cannot be exactly the same. However, it is often assumed that, they have reasonably symmetrical performance levels. The slew rate of voltage-mode and current-mode circuits is compared

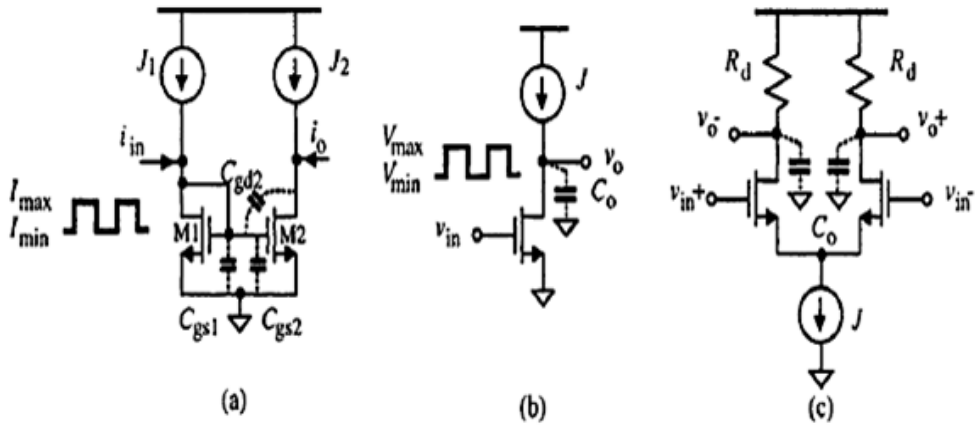

Figure 2.14: Slew rate comparison of voltage-mode and current-mode circuits (a) Basic current mirror; (b) Common-source amplifier; (c) Basic differential pair.

using the common-source configuration and the basic current mirror shown in figure 2.14. When a square waveform current is applied to the basic current mirror, because M_1 is in saturation, i_{DS1} is independent of v_{DS1} when the channel length modulation is neglected. The rate of the change of the output current depends upon how fast $C_(gs1 \sim 2) = C_gs1 + C_gs2$ is charged or equivalently how fast the gate voltage of $M1 \sim 2$ rises. Since,

$$C_{gs1\sim2}\frac{dv_{GS1\sim2}}{dt} + \frac{1}{2}\mu_n c'_{ox}(\frac{W}{L})_1(v_{GS1\sim2} - V_T)^2 = J_1 + i_{in}$$

For voltage-mode circuits, the slew rate is usually determined by the output stage because of the large width of the transistors in the output stage and the large capacitance of the load. Consider the common-source amplifier, when a sufficiently low

voltage V_{min} is applied to the input, the transistor switches off and C_o is charged by J only, we have $\left[\frac{dv_o}{dt}\right]_{rise,max} = \frac{J}{c_o}$. When $v_{in} = V_{max}$, C_o is discharged via the transistor with the slew rate $\left[\frac{dv_o}{dt}\right]_{fall,max} = \frac{1}{R_{on}c_o}$ where R_{on} is the channel resistance of the transistor in the triode. The preceding results reveal that the slew rate of common-source amplifier is set by the biasing current, the width of the transistor, and the output capacitance. It is independent of the amplitude of the input voltage.

2.4.4 propagation delay

For digital circuits, the average propagation delay is a widely used figure-of-merit depicting the transient behaviour of the circuits. It is directly related to the swing of the signal. Neglecting the resistance and the inductance, the average rising (falling) time of the voltage of a node, denoted by Δt is determined from,

$$C_n(\Delta V_n) = \int_0^{\Delta t} i(t)dt = I_{avg}\Delta t$$

where I_{ave} is the average current charging/discharging the node, C_n is the capacitance of the node, i(t) is the net current flowing into/out of the node and Δv_n is the voltage swing of the node. The above equation reveals that, a small propagation delay can be achieved by either minimizing the swing of the voltage of the node or maximizing the current charging and discharging the capacitance of the node. Unlike

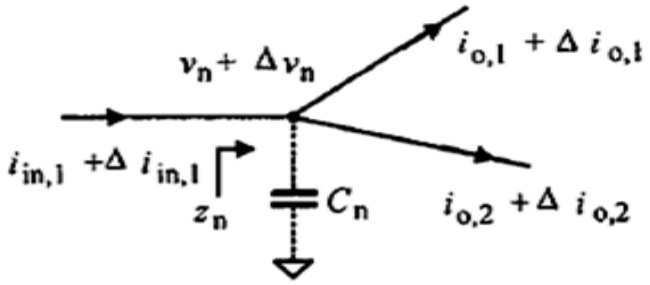

Figure 2.15: Variation of nodal voltages and branch currents of current-mode circuits.

voltage-mode circuits, the information carriers of current-mode circuits are branch currents. The variation of nodal voltages can be kept small as long as the current of

the branches associated with the nodes is large. Consider figure (2.15):

$$\Delta V_n = z_n \left(\sum_{b_1=1}^{B_1} \Delta i_{in,b_1} - \sum_{b_2=1}^{B_2} \Delta i_{o,b_2} \right)$$

where Z_n is the impedance of the node, B_1 and B_2 are the number of input and output branches connected to the node, respectively.

We conclude that for a given Δv_n, a large current variation can be obtained as long as Z_n is kept small. The small nodal voltage variation of current mode circuits lowers the amount of time needed to charge/discharge C_n, resulting in a faster transient response [21]. This is one of the key advantages of current-mode circuits.
Other important considerations are,

- The effect of V_{DD} and ground fluctuations on the output voltage or current of CMOS circuits is of a great concern in mixed-mode circuits because both analog and digital circuits often share the same supply voltage and ground. Supply voltage sensitivity, is a measure of the effect of the variation of the supply voltage on the response of the circuits.

- The oxide thickness t_{ox} is scaled down aggressively in deep submicron CMOS processes. This results in large number of electrostatic discharge(ESD) induced damages of MOSFETs mainly due to the breakdown of the gate oxide insulator.

2.4.5 High Current Gain Stages

To be able to understand the principle of high-current-gain amplifiers better, a brief description of the principles of both current-mode amplifiers and high-gain voltage amplifiers will be given in the following paragraphs.

A. Gain of Current Mode Amplifiers In figure 2.16, the simplest current-mode amplifier based on a Widlar current mirror is shown. It is obvious that if a high gain is desired, the transistors Ml and M2 must have very different sizes so that the division of their aspect ratios gives the high gain. So, for example, if the final current gain is $A_i = 100 = 40dB$, the respective dimensions of the transistors from fig 2.16 (a) must be $WM2 = 100WM1$ and $LM_1 = LM_2$, or $WM_2 = 10WM_1$ and $LM_1 = 10LM_2$ if the chip area should be minimized [31, 32]. However, if high

accuracy of the current gain is required the channel width of$M_2(WM_2)$ must not be increased, but a respective number of parallel transistors with the same channel dimensions must be used, like illustrated in fig 2.16 (b), where the gain A_i is identical with the number of the used transistors n. This low current gain drawback of current-mode amplifiers could be solved by high- current-gain amplifiers based on a different principle of current amplification [18, 26].

B. Gain Stages of voltage Amplifiers

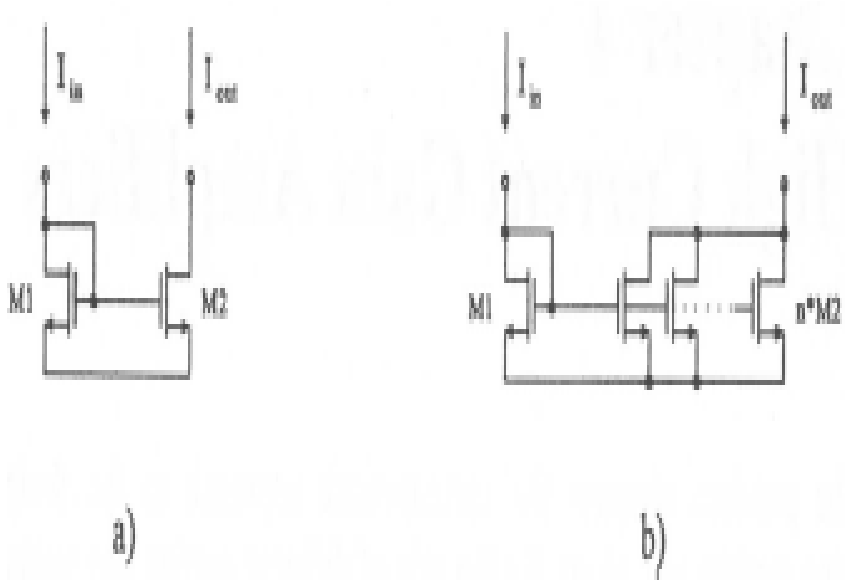

Figure 2.16: Simple current-mode amplifier, the Widlar current mirror a) with scaled dimensions b) with multiple transistorM_2 .

The basic principle of operation of high-gain voltage amplifiers can be explained by means of the voltage gain stage shown in figure 2.17 [18]. The small-signal input voltage connected to the gate transistor of M_1 is converted to the drain current of M_1 by the gate transconductance of M_1

$$i_d = g_{mM1} V_{in} \tag{2.4.9}$$

If the drain ofM_1 is loaded by a high impedance, the load transistor ofM_2, the drain

current of M_1 is converted back to voltage,

$$v_{out} = \frac{i_d}{g_{dsM1} + g_{dsM2}} = i_d r_t, \tag{2.4.10}$$

where r_t is the resistive part of the impedance of the high-impedance (transimpedance) node T.
The final small-signal voltage gain can then be expressed as,

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_{mM1}}{g_{dsM1} + g_{dsM2}} \tag{2.4.11}$$

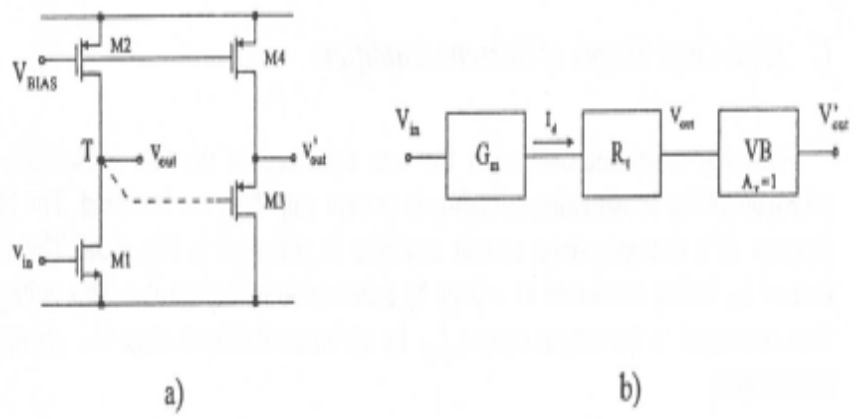

Figure 2.17: Voltage amplifier: a) CMOS implementation b) block diagram.

A voltage amplifier often needs a low-impedance output to be able to drive low-impedance or multiple loads without degrading the gain of the amplifier. Therefore, in MOS technology unity- gain amplifiers, voltage followers, voltage buffers are needed. In fig 2.17 (a) this is accomplished by the buffer transistor M_3 connected to the output of M_1 by the dashed line and the current source M_4, giving low output resistance. The resulting gain is then given by

$$A_v = \frac{v_{out}}{v_{in}} = G_m R_t, \tag{2.4.12}$$

where G_m is the transconductance of the transconductance stage and R_t is the resistance of the transresistance stage of the amplifier. If the input-output voltage transfer

of the voltage buffer is not unity, its gain (attenuation) has to be multiplied by the gain of the high-gain stage $G_m - R_t$ to obtain the overall gain of the voltage amplifier

$$A_v = \frac{v_{out}}{v_{in}} = G_m R_t A_{vb} \tag{2.4.13}$$

where A_{vb} is the input-output transfer function of the voltage buffer at the output.

C. High-Gain Stages of Current Amplifiers

Following a scheme similar to the one described in the last subsection, the principles of the construction of high-gain current amplifiers can be found. The block diagram of a one gain- stage current amplifier is presented in figure 2.18(a). The input current I_{in} is first converted to voltage by a transresistance stage R_t . This voltage is then converted to the output current I_{out} by a transconductance stage G_m giving the current gain,

$$A_i = \frac{i_{out}}{i_{in}} = G_m R_t \tag{2.4.14}$$

If a current buffer is used in order to obtain a low-impedance input, the final current gain is given by,

$$A_i = \frac{i_{out}}{i_{in}} = G_m R_t A_{cb} \tag{2.4.15}$$

where A_{cb} is the input-output current transfer function of the input current buffer. This principle was used by Bruun in his first attempt to design a high-gain current operational amplifier based on current conveyors in 1991 [19, 33].

A one gain- stage current amplifier is drawn in figure 2.19. The design of Bruun relies on a current-to-voltage conversion across the high, Y-terminal impedance of the current conveyor and a reverse voltage- to-current conversion across the low, X-terminal impedance of the current conveyor. The achieved current gain is then given by,

$$A_I = \frac{R_y}{R_x} \tag{2.4.16}$$

This technique of current amplification allowing a gain of more than 40dB for standard CMOS processes was generalized in 1992 by Zele et.al. [20]. They showed a current-gain stage, given in fig 2.18(b), based on a common-source transistor M_1 biased by the constant current source M_2. The small-signal input current i_{in} is here converted to voltage across the high output resistance of the current source r_0,

$$v_{in} = i_{in} r_o \tag{2.4.17}$$

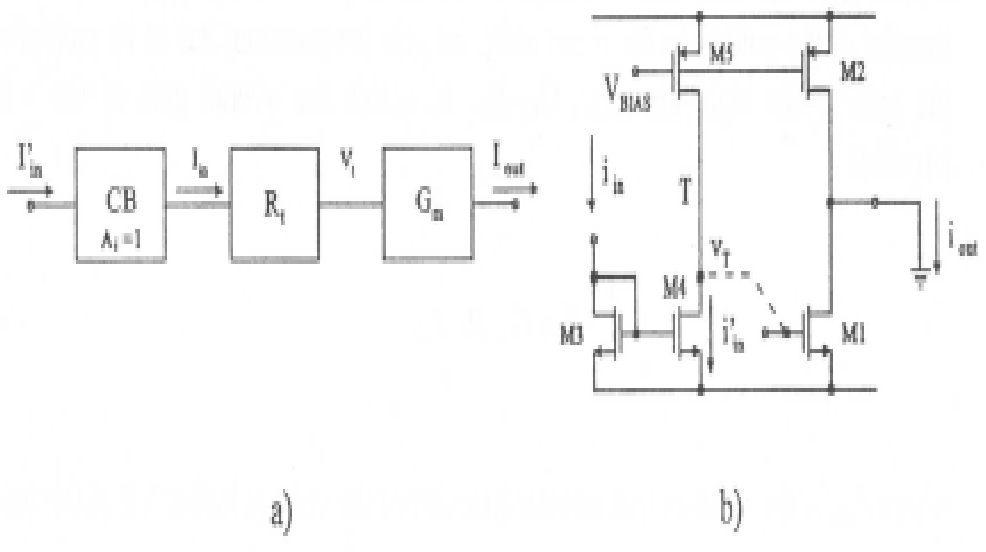

Figure 2.18: Current amplifier: a) block diagram b) CMOS implementation [18].

where r_0 is usually the function of the drain-source transconductances of the output transistors of the current source given by,

$$r_o = \frac{1}{\sum g_{ds}} \tag{2.4.18}$$

The contribution of the input of M_1 to the conversion can be neglected because of the very high gate resistances of MOS transistors. This voltage is then converted back to current via the gate transconductance of the common-source transistor M_1. By grounding the output terminal, the output current is given by,

$$I_{out} = V_{in} g_{mM1} = i_{in} r_o g_{mM1}, \tag{2.4.19}$$

The final small-signal gain of this current amplifier is then given by,

$$A_i = \frac{i_{out}}{i_{in}} = \frac{g_{mM1}}{g_{dsM4} + g_{dsM5}}, \tag{2.4.20}$$

where the sum of $g_{dsM4} + g_{dsM5}$ represents the drain-source transconductances of the output transistors of the current source.

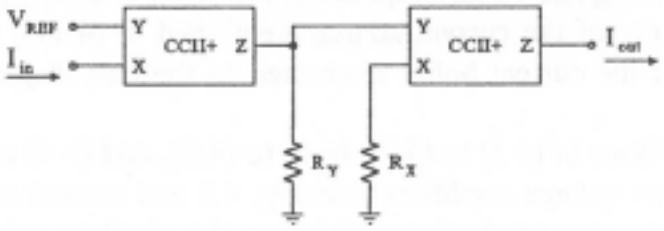

Figure 2.19: Current conveyor implementation of a current operational amplifier.

2.4.6 Transconductance and Transimpedance Amplifier

Conventional op-amps are primarily voltage amplifiers in which the output voltage equals the gain times the input voltage. The operational transconductance amplifier (OTA) is primarily a voltage-to-current amplifier in which the output current equals the transconductance times the input voltage [28]. The transconductance of an electronic device is the ratio of the output current to the input voltage. For an OTA, voltage is the input variable and current is the output variable. The transconductance, g_m is given by

$$g_m = \frac{I_{out}}{V_{in}} \tag{2.4.21}$$

Transimpedance amplifiers are operational amplifiers used to convert an input current into an output voltage. These current-to-voltage converters are useful in many important applications.

2.5 Low voltage design considerations in analog CMOS

2.5.1 Low Voltage Techniques

The reduction of the total supply voltage in CMOS integrated circuits has forced analog designers to find solutions for device that are able to operate in a wide supply range in order to obtain an acceptable signal to noise ratio. There are three possible approaches to achieve high performance analog circuits in CMOS technology at low power supply voltages [18]. One is to multiply the lower voltage dc to larger values.

Another is to modify existing CMOS technologies to accommodate low-voltage analog circuits. A third is to develop new circuit techniques that achieve this objective with existing technology [7, 16, 26, 34].

2.5.2 Classification of low voltage circuits

The classification of low voltage circuits is determined by the number of stacked gate and saturation voltages [14]. The term low voltage is used for circuits that are able to operate at a supply voltage of two stacked gate-source voltages and two saturation voltages:

$$V_{sup;min} = 2(V_{GS} + V_{Dsat}) \tag{2.5.1}$$

We also have circuits that only need a minimum supply voltage of one gate source voltage and one saturation voltage. Such circuits are referred to as extremely or ultimate low voltage circuits. This is expressed by,

$$V_{sup;min} = V_{GS} + V_{Dsat} \tag{2.5.2}$$

As we can see from the above equations, the ultimate low-voltage circuits need a supply voltage which is about half the supply voltage for low voltage circuits.

2.6 Basic Building Blocks (not only) for Current Mode Circuits

Current-mode circuits have been gaining the attention of analog designers over the last decades as an important class of analog circuits. Using current as the medium of signal processing allows to influence the power supply rejection ratio as well as to set the signal range more effective than it is done in voltage processing circuits, where the maximal signal range is solidly given by the size of the supply voltage. The key performance feature of current-mode circuits is however their inherent wide bandwidth capability [7]. This is due to the fact that, current-mode circuits do not include any internal high-impedance node and because of this, all poles and zeroes of their transfer functions lie very high on the frequency axis, approaching the f_Ts (transition frequency) of transistors in the used technology [18].

2.6.1 General Properties of Current Mirrors

A current mirror is an element with at least three terminals. The common terminal is connected to a power supply, and the input current source is connected to the input terminal. Ideally, the output current equal to the input current multiplied by a desired current gain. If the gain is unity, the input current is reflected to the output, leading to the name current mirror. Under ideal conditions, the current-mirror gain is independent of input frequency, and the output current is independent of the voltage between the output and common terminals. Furthermore, the voltage between the input and common terminals is ideally zero because this condition allows the entire supply voltage to appear across the input current source, simplifying its transistor-level design. More than one input and/or output terminals are sometimes used. In practice, real transistor-level current mirrors suffer many deviations from this ideal behavior. For example, the gain of a real current mirror is never independent of the input frequency [1, 8, 26].

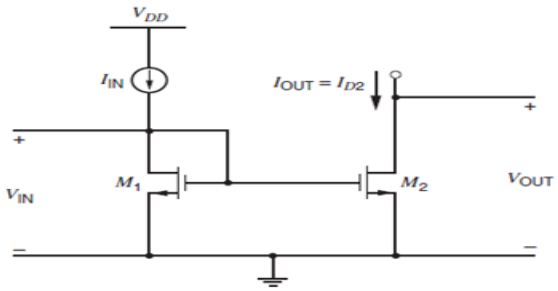

Figure 2.20: A simple MOS current mirror.

Figure 2.20 shows an MOS version of the simple current mirror. The drain-gate voltage of M_1 is zero; therefore, the channel does not exist at the drain, and the transistor operates in the saturation or active region if the threshold is positive. Although the principle of operation for MOS transistors does not involve forward biasing any diodes, M_1 is said to be diode connected in an analogy to the bipolar case. Assume that M_2 also operates in the active region and that both transistors have infinite output resistance. Then I_{D2} is controlled by V_{GS2}, which is equal to V_{GS1} by KVL. A KVL equation is at the heart of the operation of all current mirrors.

2.6.2 Ideal Current Mirror

The development in computers and communications requires much smaller chip size with low power and wide dynamic range [7]. Hence, low power and low voltage mixed mode circuits and analog are of a great importance. A series of current mirror circuit useful for low voltage analog circuit design are required to reduce channel length modulation and offering much higher accuracy [8, 10].

Chapter 3

Schematic Layout and Mathematical Formulations

3.1 Schematic layout

The schematic layout of the COA is shown in figure 3.1.

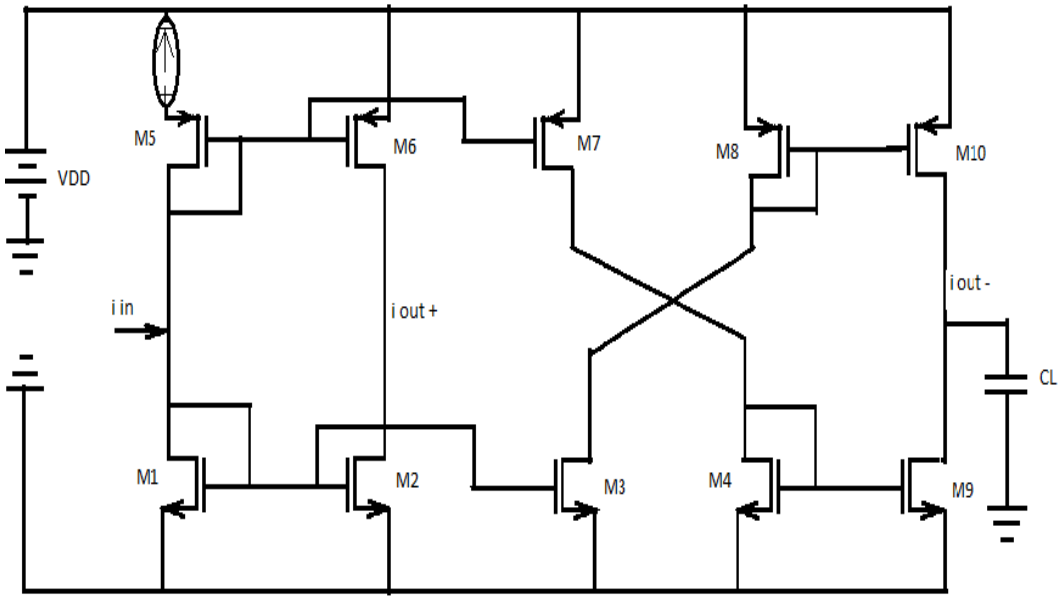

Figure 3.1: Schematic diagram of Current Operational Amplifier.

3.2 Specification

The configuration shown in figure 3.1 is the current-mode counterpart of the traditional voltage operational amplifier (VOA). The required specifications under normal operation are given in table 3.1.

Table 3.1: Specification in the current mode study

Power Supply	0and 1.5V
Open Loop Current Gain	$>$ 2dB
Unity Gain Frequency	$>$50KHz
GBW (3dB) Frequency	$>$15KHz
Phase Margin	$>$ 55degrees
Load Capacitance	100μF
CMRR	$> 20dB$
Power Dissipation	$< 10mW$
Slew Rate	$\geq 25\mu A/\mu s$
ICMR (Min, Max)	0V to 1.2V
Input/Output Current Swing	$\pm 20\mu A$

3.3 Mathematical formulation

The ideal current mirror is a two-port having a low-impedance (ideally zero ohm) grounded input terminal capable of accepting the input current I_{IN} and a high impedance output terminal (ideally approaching infinity) into which a replication of the input current, the output current I_{OUT} is forced to flow to. The sum of the input current I_{IN} and the output current I_{OUT} flows into a common node, which is usually grounded to the negative supply voltage. If current mirrors built of either n-channel or p-channel MOS transistors are employed only single polarity input current will be transferred to the output [2].

In many cases, the input-output current transfer is unity $I_{OUT}/I_{IN} = 1$, but sometimes current gain or attenuation $A_I = I_{OUT}/I_{IN} \neq 1$ is required. This input-output current transfer rates are essentially independent of the voltage on the output

terminal and the magnitude and frequency of the transferred currents. In addition, the voltage at the input terminal remains constant over a large range of input currents.

3.3.1 A Mathematical Description of MOSFET Behavior

A mathematical description of enhancement MOSFET behavior is relatively straightforward. We actually need to concern ourselves with just 3 equations. Specifically, the drain current i_D in terms of v_{GS} and v_{DS} for each of the three MOSFET modes (i.e., Cutoff, Triode, Saturation). Additionally, we need to mathematically define the boundaries between each of these three modes. But first, we need to examine some fundamental physical parameters that describe a MOSFET device [22].
These parameters include:

$$k'\text{=Process Transconductance Parameter } \left[\frac{A}{V^2}\right] \text{ and}$$
$$\frac{W}{L}\text{=Channel Aspect Ratio}$$

- The process transconductance parameter k' is a constant that depends on the process technology used to fabricate an integrated circuit. Therefore, all the transistors on a given substrate will typically have the same value of this parameter.

- The channel aspect ratio $\frac{W}{L}$ is simply the ratio of channel width (W) to channel length (L). This is the MOSFET device parameter that can be altered and modified by the circuit designer to satisfy the requirements of the given circuit or transistor.

We can likewise combine these parameter to form a single MOSFET device parameter k, given by

$$k = \frac{1}{2}k'\left(\frac{W}{L}\right)\left[\frac{A}{V^2}\right] \tag{3.3.1}$$

Now we can mathematically describe the behavior of an enhancement MOSFET.

CUTOFF: If the MOSFET is in cutoff, the drain current is simply zero.
i.e.

$$i_D = 0 \tag{3.3.2}$$

TRIODE:
When in triode mode, the drain current is dependent on both v_{GS} and v_{DS} given by,

$$i_D = k' \left(\frac{W}{L}\right) \left[(V_{GS} - V_{Th})V_{DS} - \frac{1}{2}V_{DS}^2\right] \tag{3.3.3}$$

$$i_D = k \left[2(V_{GS} - V_{Th})V_{DS} - V_{DS}^2\right] \tag{3.3.4}$$

This equation is valid for both NMOS and PMOS transistors (if in triode mode). Recall that, for PMOS devices, the values of v_{GS} and v_{DS} are negative, but note that this will result (correctly so) in a positive value of i_D.

SATURATION:
When in saturation mode, the drain current is (approximately) dependent on V_{GS} only.

$$i_D = \frac{1}{2}k' \left(\frac{W}{L}\right) (V_{GS} - V_{Th})^2 \tag{3.3.5}$$

$$i_D = k(V_{GS} - V_{Th})^2 \tag{3.3.6}$$

where $k = \frac{1}{2}k' \left(\frac{W}{L}\right)$.
Thus, we see that, the drain current in saturation is proportional to excess gate voltage squared.

Parameters of an Op-Amp

This section will discuss Op-Amp parameters. The selection of any op-amp must be based on an understanding of what particular parameters are most important to the application [25, 3].

Offset Voltage:
All op-amps require a small voltage between their inverting and non inverting inputs to balance mismatches due to unavoidable process variations. The required voltage is known as the input offset voltage and is abbreviated, V_{os}. V_{os} is normally modelled as a voltage source driving the noninverting input. Generally, Bipolar input op-amps typically offer better offset parameters than JFET or CMOS input op-amps. Input offset voltage is of concern anytime that DC accuracy is required of the circuit. One way to null the offset is to use external null resistors on a single op-amp package. A potentiometer is connected between the null inputs with the adjustable terminal connected to the negative supply through a series resistor. The input offset voltage is nulled by shorting the inputs and adjusting the potentiometer until the output is zero. However, even if the V_{os} is nulled at the beginning, it will change with temperature and some other conditions [25, 34].

Input Current:
The input circuitry of all op amps requires a certain amount of bias current for proper operation [34]. The input bias current, I_{IB}, is computed as the average of the two inputs:

$$I_{IB} = \frac{(I_N + I_P)}{2} \tag{3.3.7}$$

CMOS and JFET inputs offer much lower input current than standard bipolar inputs.

The difference between the bias currents at the inverting and noninverting inputs is called the input offset current, $I_{IO} = I_N - I_P$. Offset current is typically an order of magnitude less than bias current. Input bias current is of concern when the source impedance is high. If the op-amp has high input bias current, it will load the source and a lower than expected voltage is seen [4]. The best solution is to use an op-amp with either CMOS or JFET input. The source impedance can also be lowered by using a buffer stage to drive the op-amp that has high input bias current.

In the case of bipolar inputs, offset current can be nullified by matching the

impedance seen at the inputs. In the case of CMOS or JFET inputs, the offset current is usually not an issue and matching the impedance is not necessary.

Input Common Mode Voltage Range(ICMR):
The input common voltage is defined as the average voltage at the inverting and non inverting input pins. If the common mode voltage gets too high or too low, the inputs will shut down and proper operation ceases. The common mode input voltage range (ICMR), specifies the range over which normal operation is guaranteed. For instance, rail to rail input op-amps use complementary N and P channel devices in the differential inputs. When the common-mode input voltage nears either rail, at least one of the differential inputs is still active, and the common-mode input voltage range includes both power rails [34, 6].

Each of the two input pins of the op-amp has voltage swing restrictions. These restrictions are due to the input stage design. In the device product data sheet, the input voltage restrictions are clearly defined in one of two ways. Most commonly, the input voltage range, V_{IN}, is specified as a separate line item in the specification table. This specification is also usually defined as a condition for the CMRR specification, input common-mode voltage range, V_{CM}. The more conservative specification of the two is where the input voltage range is called out as a CMRR test condition because the CMRR test validates the input voltage range with a second specification [35]. The input voltage range is more a function of the input circuit topology rather than the silicon process.

Maximum Output Voltage Swing:
The maximum output voltage, V_{OM}, is defined as the maximum positive or negative peak output voltage that can be obtained without waveform clipping, when quiescent DC output voltage is zero. V_{OM} is limited by the output impedance of the amplifier, the saturation voltage of the output transistors, and the power supply voltages [34].

Common-Mode Rejection Ratio:
Common-mode rejection ratio, CMRR, is defined as the ratio of the differential voltage amplification to the common-mode voltage amplification, $\frac{A_{DM}}{A_{CM}}$. Ideally this ratio would be infinite with common mode voltages being totally rejected. The common-mode input voltage affects the bias point of the input differential pair [34, 36, 37].

Supply Voltage Rejection Ratio:
Power supply rejection ratio (PSRR) is the ratio of power supply voltage change to output voltage change. The power supply rejection ratio specification quantifies the amplifiers sensitivity to power supply changes. Ideally, the power supply rejection ratio should be infinite. Typical specifications for a power supply rejection ratio of an amplifier range from 60dB to 100dB.

As with the open loop gain (A_{OL}) characteristics of an amplifier, DC and lower frequency power supply noise is rejected more than at higher frequencies. In a closed loop system, a less than ideal power supply rejection capability of an amplifier manifests itself as an offset voltage error ($PSRR_{ERROR} = \Delta V_{OS}$) [34, 38].

This error is best described with the following formula:

$$PSRR(dB) = 20log(\Delta V_{SUPPLY}/\Delta V_{OS}) \tag{3.3.8}$$

The formula that describes power supply rejection is:

$$PSR(V/V) = \Delta V_{OS}/\Delta V_{SUPPLY} \tag{3.3.9}$$

where:$V_{SUPPLY} = V_{DD} - V_{SS}$ and ΔV_{OS}= input offset voltage change due to PSR

Slew Rate:
Slew rate (SR) is the maximum output voltage rate (either positive or negative). Its

units are V/ms or V/μs [6,34] and caused by ,

$$I_{out} = C_L \frac{dv}{dt} \tag{3.3.10}$$

When I_{out} is constant, the rate is constant. Generally the slew rate can only occur when the differential input signal is large enough to cause I_{SS} (I_{DD}) to flow through only one of the differential input transistors.

$$SR = \frac{I_{SS}}{C_L} = \frac{I_{DD}}{C_L} \tag{3.3.11}$$

Figure 3.2 shows slew rate graphically. The primary factor controlling slew rate

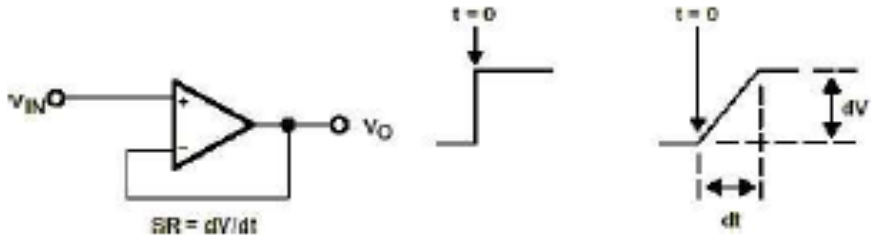

Figure 3.2: Slew rate

in most amplifiers is an internal compensation capacitor C_C, which is added to make the op-amp unity gain stable. Voltage change in the second stage is limited by the charging and discharging of the compensation capacitor C_C. However, that not all op-amps have compensation capacitors. In op-amps without internal compensation capacitors, the slew rate is determined by internal op-amp parasitic capacitances. Uncompensated op-amps have greater bandwidth and slew rate, but the designer must ensure the stability of the circuit [36]. In op-amps, power consumption is traded for noise and speed. In order to increase slew rate, the bias currents within the op-amp are increased [34].

Unity Gain Bandwidth and Phase Margin (UGB and PM):
There are five parameters relating to the frequency characteristics of the op-amp that

are likely to be encountered. These are unity-gain bandwidth (UGB), gain bandwidth product (GBW), phase margin at unity gain ϕ_m, gain margin (A_m) and maximum output-swing bandwidth (B_{OM}).

Unity-gain bandwidth (UGB) and gain bandwidth product (GBW) are very similar. UGB specifies the frequency at which A_{VD} of the op-amp is 1 [].

$$UGB = (f)A_{VD} = 1 \tag{3.3.12}$$

GBW specifies the gain-bandwidth product of the op-amp in an open loop configuration and the output loaded:

$$GBW = A_{VD} \times f \tag{3.3.13}$$

GBW is constant for voltage-feedback amplifiers. It does not have much meaning for current- feedback amplifiers because there is no linear relationship between gain and bandwidth [36].
Phase margin at unity gain, ϕ_m is the difference between the amount of phase shift a signal experiences through the op-amp at unity gain and 180^0:

$$\phi_m = 180^0 - \phi@UGB \tag{3.3.14}$$

Gain margin is the difference between unity gain and the gain at 180^0 phase shift [34]:

$$Gain\ margin = 1 - Gain\ @180^0\ phase\ shift \tag{3.3.15}$$

Maximum output-swing bandwidth (B_{OM}) specifies the bandwidth over which the output is above a specified value:

$$B_{OM} = f_{MAX}, \tag{3.3.16}$$

while $V_O > V_{MIN}$

The limiting factor for B_{OM} is slew rate. As the frequency gets higher and higher, the output becomes slew rate limited and can not respond quickly enough to maintain the specified output voltage swing. In order to make the op-amp stable, capacitor, C_C, is purposely fabricated on chip in the second stage. This type of frequency compensation is termed dominant pole compensation. The idea is to cause the open-loop

gain of the op-amp to roll off to unity before the output phase shifts by 180^0. Phase margin ϕ_m and gain margin ($A_{m)}$ are different ways of specifying the stability of the circuit.

The differential mode input current (i_d) is given by:

$$i_d = (i_1 - i_2). \tag{3.3.17}$$

And the common mode input current (i_c) is:

$$i_c = \frac{i_1 + i_2}{2} \tag{3.3.18}$$

Power dissipation

The power dissipation simply implies the total power consumed by the device and is give by:

$$P_{dis} = \sum_{i=1}^{n} p_i \tag{3.3.19}$$

where n is the number of transistors and p_i is the power dissipation on each transistors.

Chapter 4

Design and Simulation

4.1 Design of Current-Mode Op-Amp Using a Class-AB Configuration

As we know a CMOS is a technology which consists of two NMOS and PMOS or n-channel and p-channel enhancement MOSFETs connected in series in the same circuit. These MOSFETs more over working complimentarily. That is, when one conducts the other will be off. At high input voltage NMOSs will on while PMOSs will be off and vice versa at low input voltage.

As its name suggests, the class AB amplifier is a combination of the class A and class B type amplifiers. The conduction angle of a class AB amplifier is somewhere between 180^0 and 360^0. In this type of amplifier both devices (n- and p- channels) are allowed to conduct at the same time around the waveforms crossover point eliminating the crossover distortion problems.

Figure 4.1 shows the circuit designed using OrCAD PSPICE simulation software. M_1 is coupled in series with M_5; M_2 is coupled in series with M_6; M_3 is cross-coupled in series with M_8; M_4 is cross-coupled in series with M_7 and M_9 is coupled in series with M10. Since cascode (connection of two transistors in common source- CS and common gate- CG configurations) converts a voltage in to a current, we can use it at the output stages. It is also advisable to introduce in the circuit to have a high output impedance.

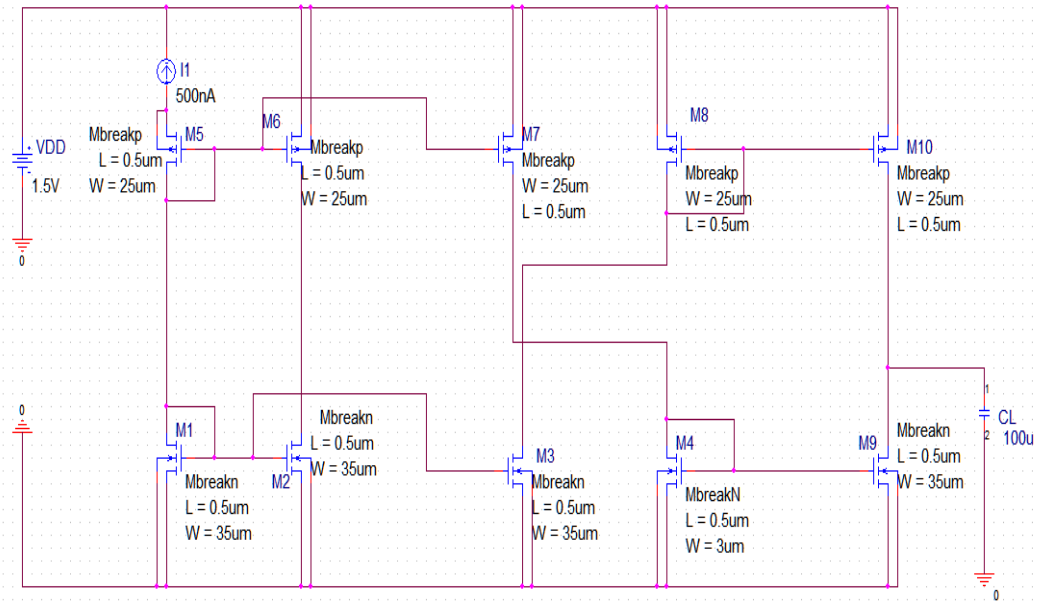

Figure 4.1: Aspect ratio or W/L for Low Voltage Class AB Current Amplifier

From figure 4.1, we can observe that, the transistor sizes have been modified through simulation for optimum performance. These values are listed in table 4.1.

4.2 DC-Analysis

In DC analysis the bias point is used to measure the operating point of the design circuit, like node voltage, node current, and power dissipation at which it can be adjusted by the input offset voltage to get minimum output offset voltage.

Table 4.1: Aspect ratios of Transistors used in the design.

Device	Width/Length in (μm/μm)
M_1=M_2=M_3=M_9	35/0.5
M_5=M_6=M_7=M_8=M_{10}	25/0.5
M_4	3/0.5

- **Node voltage:** It is the voltage at each junctions in the design. Figure 4.2 shows the simulation result of the node voltages and output offset voltage. The output offset voltage is 330.7pV, which is negligibly small.

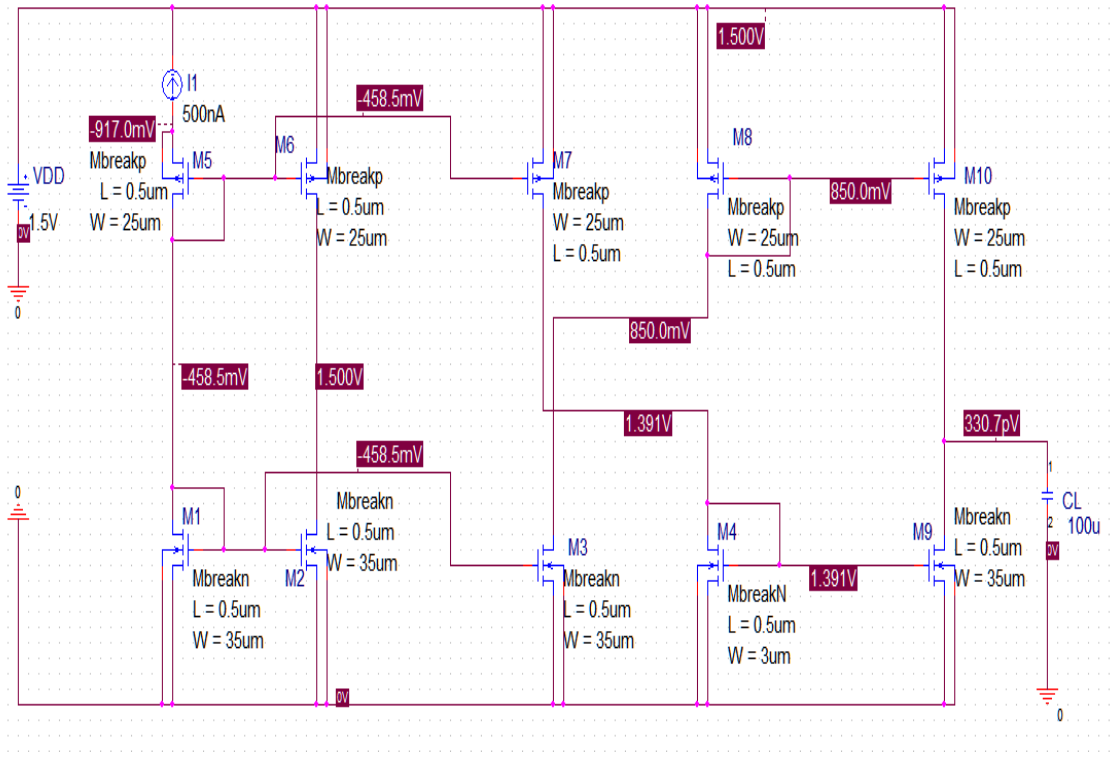

Figure 4.2: Simulation of Node Voltages and Output offset Voltage

- **Node current:** Once the output offset voltage is adjusted by input offset voltage, it is simple to determine the node currents. The node current simulation results is shown in figure 4.3.

I_{D1}=$-I_{D5} = 500nA$; I_{D2}=$-I_{D6} = 1.51pA$; $I_{D3} = 860fA$; I_{D4}= $-I_{D7}$=164.7μA; $I_{D8} = -904.9fA$; $I_{D9} = 1.71pA$; $I_{D10} = -1.755pA$

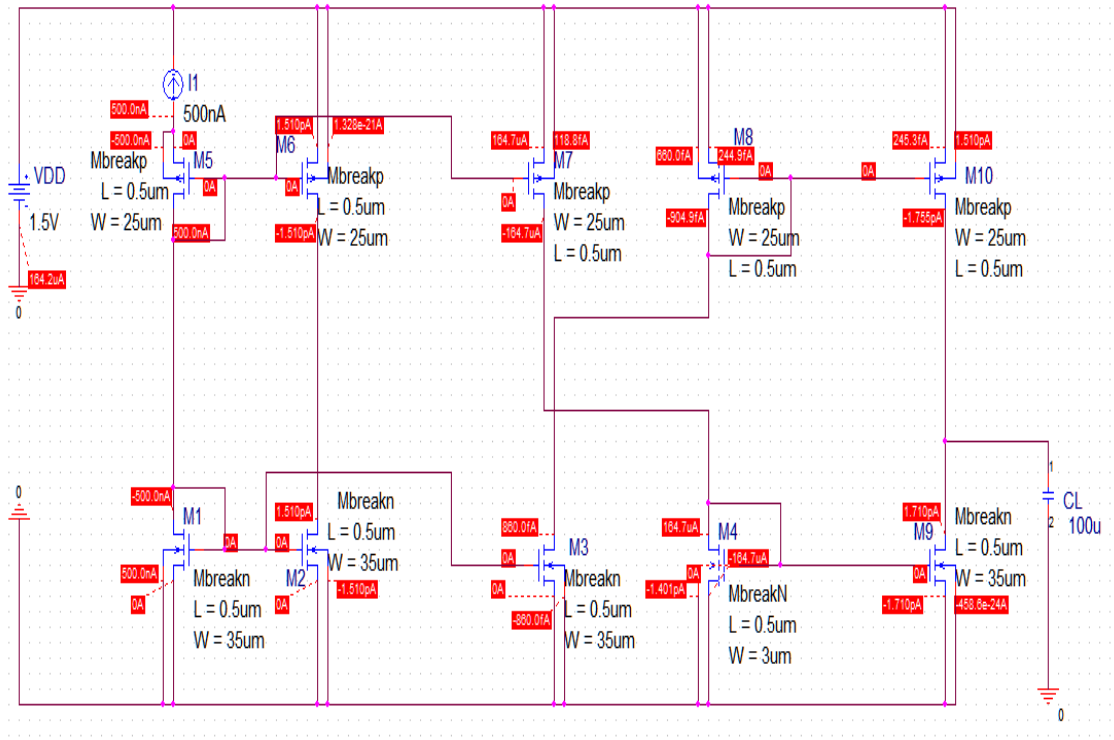

Figure 4.3: Simulation of Node currents

- **Power Dissipation:** The power consumed by each transistor is shown in figure 4.4. And the total power dissipation is given by:

$P_{Total\ diss}$=229.1μW+17.95μW-1.209μW+229.3nW+229.3nW+2.265pW+2.633pW +731fW+588.2fW+1.446x10^{-21}W+565.6x10^{-24}W
$P_{Total\ diss}$=0.246mW

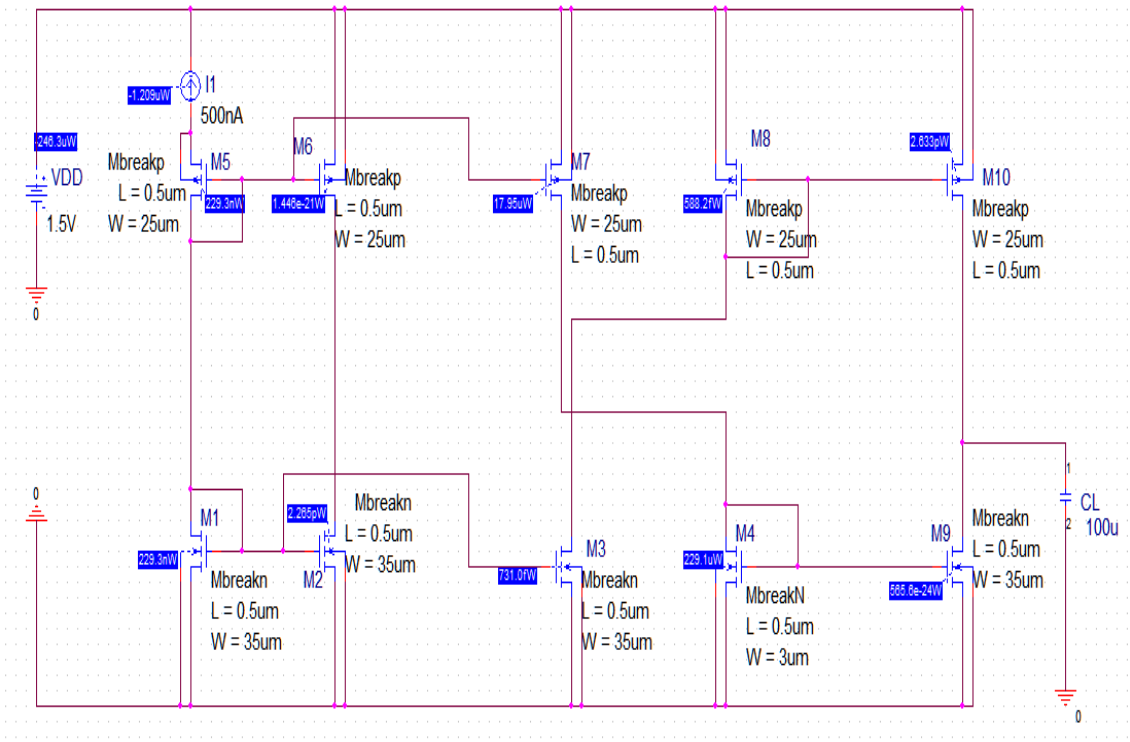

Figure 4.4: Simulation of Power Dissipation

4.2.1 DC Sweep

Input Common Mode Range (ICMR):

The input common mode range is the range of DC common mode input voltage for which an op amp behaves normally with its key parameters, including offset voltage and input bias current. It is the maximum input voltage range that all transistors are able to work in saturation. The DC analysis is used to calculate the state of circuit elements with fixed (time independent) input(s) after an infinite period of time, that is, DC sweeps steadily the state of voltage, current and other digital systems when sweeping as source model parameter over a range of value. The circuit design for the ICMR is shown in figure 4.5.

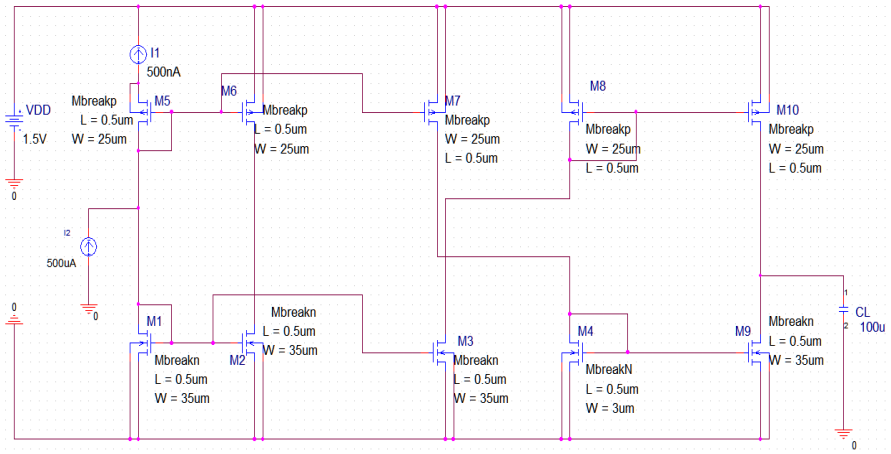

Figure 4.5: Design of ICMR

Figure 4.6 shows the simulation result for the ICMR. We can see that the ICMR ranges from 117.207mV to 1.2176V.

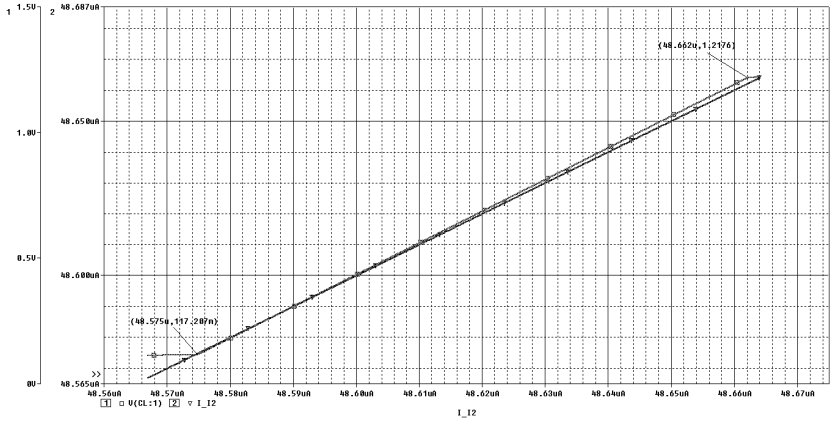

Figure 4.6: Simulation Result for ICMR

4.3 AC-Analysis

4.3.1 Time Domain/Transient Analysis:

AC sources are time dependent and the circuit has input small signals as a function of frequency applied to the input terminal(s). The output value of the AC signal varies over a range of frequencies in phase or out of phase with the input values of AC signal. Transient (time domain) analysis is probably the most popular analysis.

- AC Sweep

Open loop gain: The circuit design for the open loop gain is shown in figure 4.7. The open loop gain, gain bandwidth and unity gain frequency are obtained from AC sweep analysis. An AC current source of 1A-amplitude is connected to the noninverting input terminal.

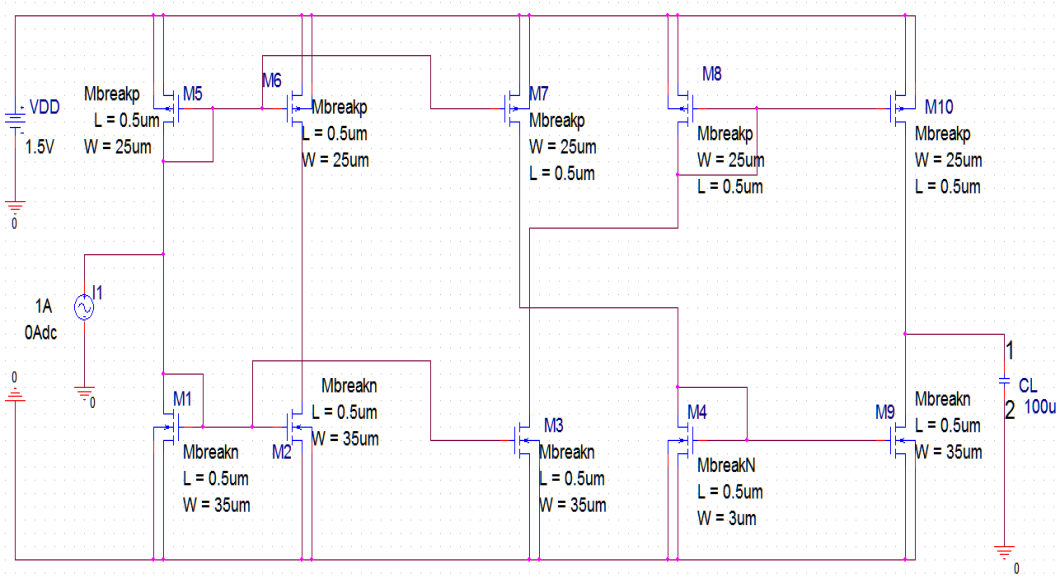

Figure 4.7: Design of Open loop gain

Figure 4.8 shows the simulation result for the open loop gain and phase margin. From the figure we can observe that the open loop gain is 8.8528dB, the GBW (3dB) frequency is 32.43KHz, and the unity gain frequency is 67.365KHz. The phase margin is 120 degrees.

Common mode gain:
The design for common mode gain is shown in figure 4.9. A 5μA- peak AC current was connected as input signal.

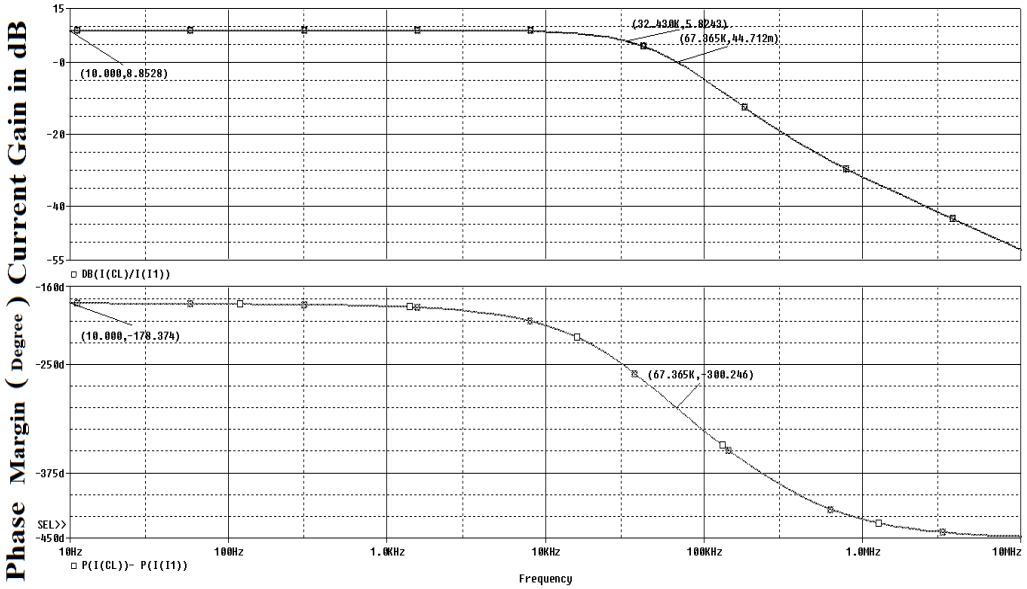

Figure 4.8: Simulation of Open loop gain

From figure 4.10 we can observe that the simulation result for the common mode rejection ratio (CMRR) is 21.127dB.

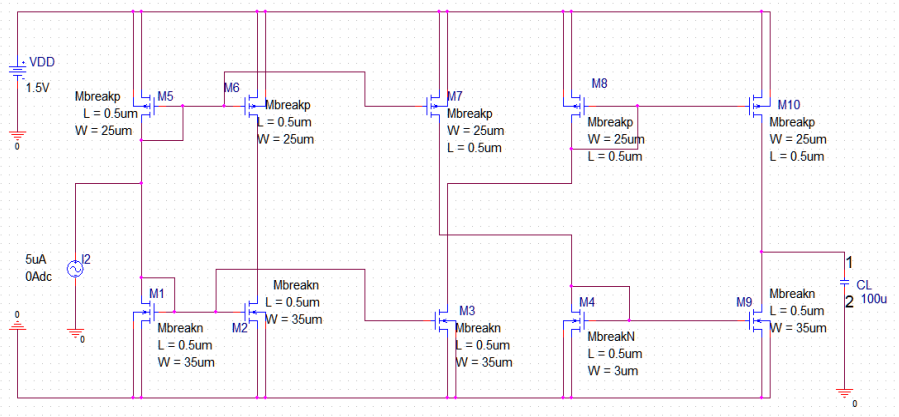

Figure 4.9: Design of CMRR

Input/Output Current Swing:
The input/output current swing design is shown in figure 4.11. A sinusoidal input current signal of 20μA is connected to the noninverting terminal to determine the output current swing.

From the simulation result shown in figure 4.12, the input current swing is from -19.993μA to 20μA and output current swing is from -15.078μA to 18.103μA.

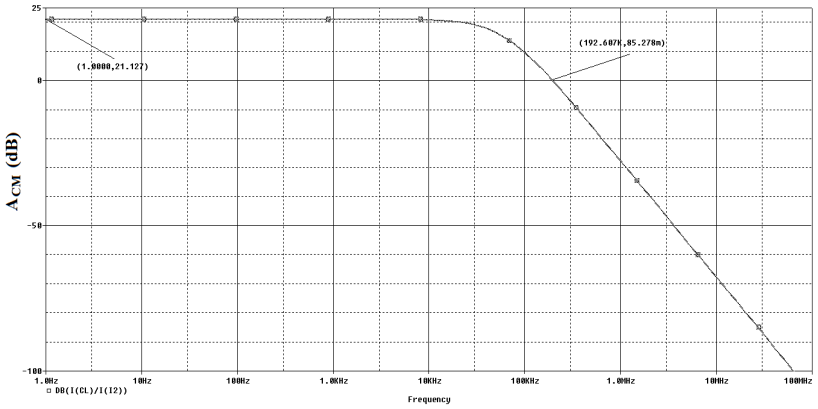

Figure 4.10: Simulation of CMRR

Slew Rate:

The slew rate can be determined from the slope of the out put waveform during the rise or fall of the output when an input signal of 5μA-amplitude pulse having 10ms period is applied on the noninverting terminal of the differential pair, while the inverting terminal is connected to the output terminal with out any ground, as shown in figure 4.13.

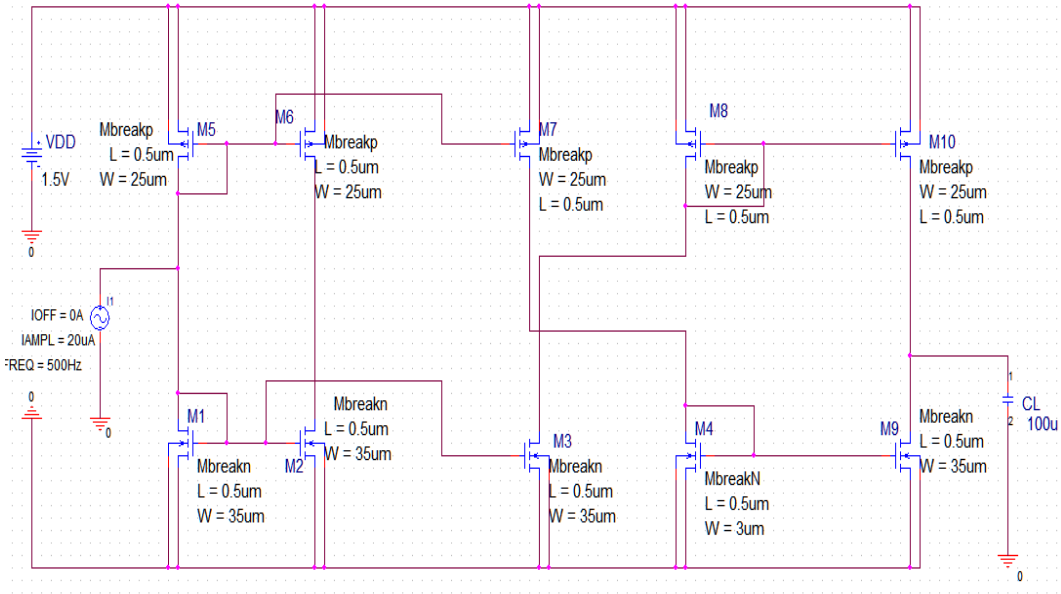

Figure 4.11: Design of Input/Output Current Swing

The simulation result of the slew rate is shown in figure 4.14. We can observe that the slew rate is 21.46A/s.

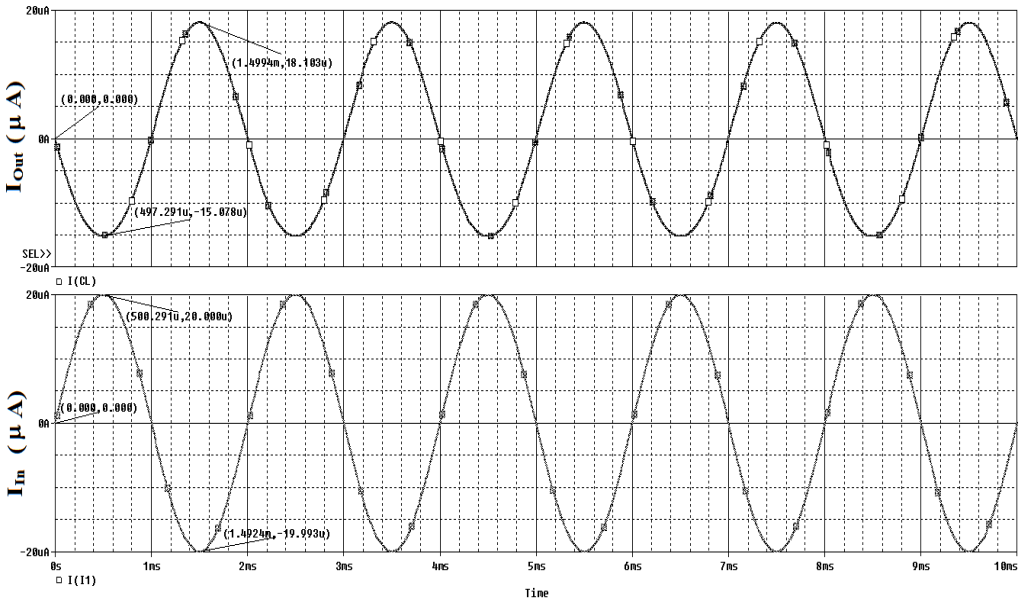

Figure 4.12: Simulation of Input/Output Current Swing

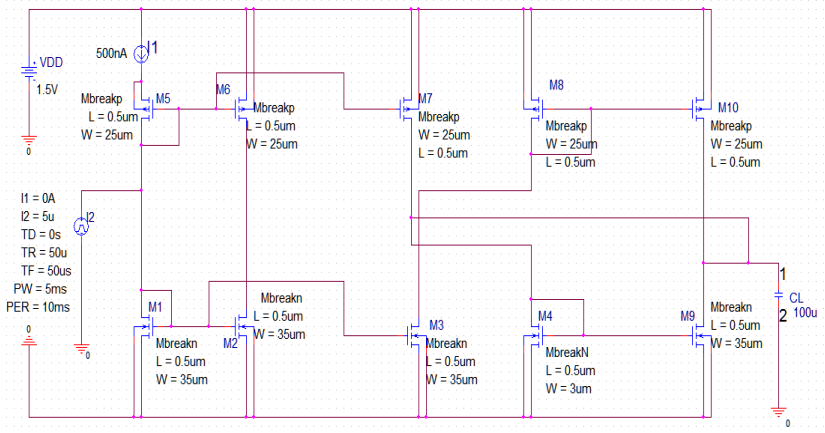

Figure 4.13: Design of Slew Rate

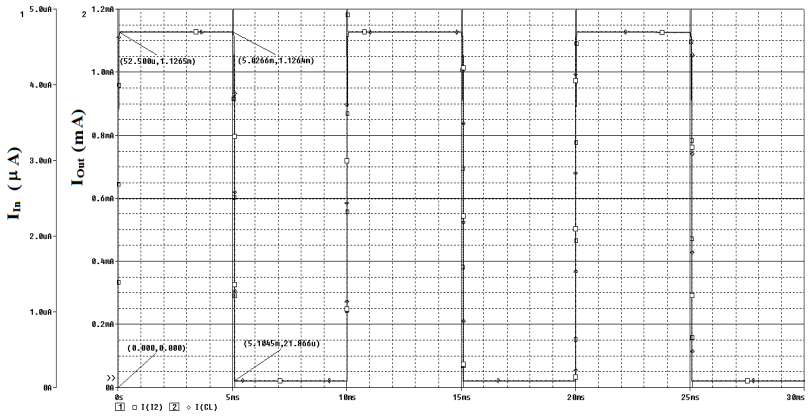

Figure 4.14: Simulation of Slew Rate

Chapter 5

Conclusion and Scope for Future Work

5.1 Conclusions

In certain practical circuit applications of CMOS op-amps, we have seen that the current-mode analogue signal processing has advantages over voltage mode processing. Generally, the current-mode processing offers high-performance properties such as wide bandwidth and accuracy. Furthermore, these circuits are potentially operated with low supply voltages.

In this research work, an innovative way of designing a low voltage class AB CMOS op-amp was developed, featuring the standard CMOS technology and 1.5 volt supply. Based on the results obtained from simulations, we can conclude that, the design has achieved its objectives because of the following performance characteristics.

- Our design has improved the open loop gain is more than four fold from the specification value of 2dB to 8.853dB. The GBW and unity gain frequency were improved by 116.2% and 34.7%, respectively.
- The phase margin result from the design is 120^0. This is enhanced by 118.2% from the specification value of 55^0.
- The CMRR of the circuit designed in this study is slightly improved by 5.6%.

- The Slew rate simulation result is 85.8% of the specification value. This needs slight improvement.
- The peak-to-peak output AC current swing was found to be 33.2μA, while the peak-to-peak input AC current swing was 39.993μA. This is 83% of the specification value. This needs further improvement.
- The ICMR result is from 1.1V. This is 91.7% of the specification value.
- The power consumed by the circuit was found to be 0.246mW. This is a reduction of power dissipation by 97.5% of the specification value of 10mW.
- The output offset voltage is 330.7pV, which is very negligible..

5.2 Scope For Future work

In this research work, we have observed that some performance parameters have slightly lower values than the specification values. So, in the future we will investigate to improve the input/output current swing, ICMR, and the slew rate.

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Declaration

I, hereby declare that, the thesis is my original work and has not been presented for a degree in any other university and that all sources of materials have been duly acknowledged.

Name: Awoke Tsegaw Engida

Signature: _____

Date: _____

This thesis has been submitted for examination with my approval as a University advisor.

Name: Dr Haileeyesus Workineh

Signature: _____

Date: