2026-06-29

A Comparative Analysis of A Three-Stage Cmos Op-Amp and A Two-Stage Cmos Op-Amp With Current Buffer

Tadesse, Baye

A COMPARATIVE ANALYSIS OF A THREE-STAGE CMOS OP-AMP AND A TWO-STAGE CMOS OP-AMP WITH CURRENT BUFFER

A THESIS SUBMITTED TO
THE DEPARTMENT OF PHYSICS OF
BAHIR DAR UNIVERSITY

IN PARTIAL FULFILLMENT OF THE
REQUIREMENTS FOR THE DEGREE OF
MASTER OF SCIENCE IN PHYSICS

By

Tadesse Baye

BAHIR DAR, ETHIOPIA
JUNE 29, 2026

Advisor:- Dr Haileeyesus Workineh

BAHIR DAR UNIVERSITY
COLLEGE OF SCIENCE
DEPARTMENT OF
PHYSICS

The undersigned hereby certify that they have read and recommend to the Faculty of Graduate Studies for acceptance a graduate thesis entitled "**A COMPARATIVE ANALYSIS OF A THREE-STAGE CMOS OP-AMP AND A TWO-STAGE CMOS OP-AMP WITH CURRENT BUFFER**" by **Tadesse Baye** in partial fulfillment of the requirements for the degree of **Master of Science in physics**.

Dated: June 29, 2026

APPROVED BY EXAMINING COMMITTEE:

Examiners:

Dr. Tizazu Abza (External Examiner)

Prof. Gebregzabher Kahsay (Internal Examiner 1)

Dr. Tamiru Nigussie (Internal Examiner 2)

Advisor:

Dr Haileeyesus Workineh

BAHIR DAR UNIVERSITY

COLLEGE OF SCIENCE

Date: **June 29, 2026**

Author: **Tadesse Baye**

Title: **A COMPARATIVE ANALYSIS OF A THREE-STAGE CMOS OP-AMP AND A TWO-STAGE CMOS OP-AMP WITH CURRENT BUFFER**

Department: **Physics**

Degree: **M.Sc.** Convocation: **June 29,** Year: **2026**

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This Thesis Work is dedicated to my family.

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Acknowledgements

First of all, thanks to God, from the bottom of my heart, who helped me in any success in my life. God is with me everywhere.

I would like to give a special thanks to my advisor and instructor Dr Haileeyesus Workineh, at the Bahir Dar University, College of Science, Department of Physics. His continuous comments, encouragement, guidance, and corrections has made the completion of this thesis work possible. Working with him has allowed me to acquire many skills as an electronics student, particularly, on Cadence OrCAD and Allegro SPB v17.4 software. I greatly respect and admire him and simply say thank you for everything.

Finally, I would like to express my thanks to all my family, especially to my intimate Sister Kalkidan for her financial support, continuous encouragement and being with me all the time.

Name: Tadesse Baye

Date:

Abbreviations Used

W/L	Aspect ratio
$\mu_{n,p}$	charge carrier Mobility
CMRR	Common Mode Rejection Ratio
CMOS	Complementary Metal Oxide Semiconductor
dB	Decibel
I_D	Drain Current
ICMR	Input Common Mode Range
GBW	Gain Bandwidth
g_m	Transconductance
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NMOS	n-Channel MOSFET
Op-Amp	Operational Amplifier
PM	Phase Margin
PMOS	p-Channel MOSFET
PD	Power Dissipation
PSRR	Power Supply Rejection Ratio
SR	Slew Rate
VLSI	Very Large Scale Integration

Abstract

Over the past decades CMOS technology has been continuously scaling and resulted in sustained improvement in transistor speeds. However, achieving higher DC open-loop gain from the op-amps became challenging. Also, the transistor threshold voltages did not decrease at the same rate as the supply voltage. This thesis work presents a detailed comparative study on the DC open loop gain and voltage swing from two different CMOS topologies: A three-stage CMOS op-amp and a two-stage CMOS op-amp with current buffer circuit. We have designed, simulated, and analyzed the two circuit topologies using industry standard Cadence OrCAD and Allegro SPB v17.4 software. The three-stage CMOS op-amp exhibited 156.55 dB, 428.67 MHz, and 67^0 as DC gain, GBW, and PM respectively. Whereas, the two-stage CMOS op-amp with current buffer circuit show 133.33 dB, 6.87 MHz, and 73.6^0 results of DC gain, GBW, and PM

Key Words: CADENCE, CMOS, GBW, Gain, Voltage Swing.

Chapter 1

INTRODUCTION

1.1 Historical Background

Operational Amplifiers (op-amps) are one of the most widely used building blocks for analog and mixed-signal systems. They are employed from DC bias applications to high speed amplifiers and filters. General purpose op-amps can be used as buffers, summers, integrators, differentiators, comparators, negative impedance converters, and many other applications. With the quick improvements of computer aided design (CAD) tools, advancements of semiconductor modelling, steady miniaturization of transistor scaling, and the progress of fabrication processes, the integrated circuit market is growing rapidly. Nowadays, complementary metal-oxide semiconductor (CMOS) technology has become dominant over bipolar technology for analog circuit design in a mixed-signal system due to the industry trend of applying standard process technologies to implement both analog circuits and digital circuits on the same chip.

While many digital circuits can be adapted to a smaller device level with a smaller power supply, most existing analog circuitry requires considerable change or even a redesign to accomplish the same feat. With transistor length being scaled down to a few tens of nanometer, analog circuits are becoming increasingly more difficult to improve upon. The classic Widlar op-amp architecture, originally developed for bipolar devices,[1] has required modification for use with CMOS devices. In particular, it has proved difficult to match the open loop gain of bipolar op-amps with CMOS technology.[2, 3] This is due to the inherently lower trans-conductance of CMOS devices as well as the gain reduction due to short channel effects that comes into play

for submicron CMOS processes.

Op-amps are one of the most critical components in analog real-time signal processing systems.[4] As integrated circuit technology continues to advance, high-performance op-amps are increasingly used in analog signal processing, sensor interfaces, data conversion, and other fields. Many configurations of current mirror are discussed and used for many applications, especially in cascade current mirror circuit which is one of the main building blocks of analog and mixed-signal integrated circuits.[5] The cascade structure, two-stage, and three-stage op-amp architectures have become focal points of recent research, aiming to achieve higher gain, better common-mode rejection ratio (CMRR), and improved output drive capability.

Invented in 1979 and subsequently refined in 1990, the CMOS active-cascade gain-enhancement technique finds wide applications in analog integrated circuits,[6] playing significant role in the study of high-gain op-amps. Because of the increasing demand to the low power systems designing of the low power circuits is taken great consideration.[7] Integrated circuits once served the role of subsystem components, portioned at analog-digital boundaries, however they now integrate complete systems on a chip by combining both analog and digital functions.[8] Complementary metal-oxide semiconductor (CMOS) technology has been the main-stay in mixed-signal because it provides density and power savings on the digital side, and a good mix of components for analog design. However, continued scaling of CMOS processes has continually challenged the established paradigm for op-amps design. Scaling down of CMOS feature sizes enable yet faster speeds, the supply voltage is scaled down to enhance device reliability and improve power consumption.

Op-amps typically are composed of either two or three stages consisting of a differential amplifier, a gain stage and an output stage. In some applications, the gain stage and the output stage are one and the same if the load is purely capacitive. However, if the output is to drive a large resistive load, then a high current gain buffer amplifier is used at the output. Each stage plays an important role in the performance of the amplifier.

1.2 Two-Stage CMOS Operational Amplifier

1.2.1 Basic Principles

Two-stage op-amps are core modules for analogue integrated circuit design, offering high gain, good stability and wide applicability. First stage (differential input stage) provides high differential gain, high input impedance and common mode rejection ratio, differential pairing tube-active loads (e.g. current mirrors) to maximize gain. The output is single-ended or differential (converted to single-ended output by current mirror). Second stage (gain level) function provides additional voltage gain and drives the output. Common source (CS) or common emitter (CE) amplifiers (for high gain), active loads (e.g. current sources or resistors), achieved by two-stage high-gain cascade, current mirrors convert differential currents to single-ended outputs. Two-stage op-amp is the cornerstone of analogue design, balancing gain, stability and versatility. Its performance depends on optimization of bias design, compensation capacitance and transistor size. Modern improved architectures (e.g. folded common-source, common-gate, sleeved op-amps) are based on this foundation.The design of a two-stage op-amp requires two stages to serve different purposes. The first stage provides high gain, while the second stage ensures output swing and stability.

Op-amps are the backbone for many analog circuits such as switched capacitor filters, algorithmic, pipelined and sigma delta A/D converter, sample and hold amplifier, etc. The speed and accuracy of these circuits depend on the bandwidth and DC gain of the op-amps. Larger the bandwidth and gain, higher the speed and accuracy of the op-amp are a critical element in analog sampled data circuit, such as SC filters, modulators.[9] The first block, in Fig.1.1, is a differential amplifier. It has two inputs which are the inverting and non-inverting inputs. It provides at the output a differential voltage or a differential current that, essentially, depends on the differential input only.

The next block is a differential to single-ended converter. It is used to transform the differential signal generated by the first block into a single ended version. Some architecture doesn't require the differential to single ended function; therefore, the block can be excluded. In most cases the gain provided by the input stages is not sufficient and additional amplification is required. This is provided by intermediate stage, which is another differential amplifier, driven by the output of the first stage.

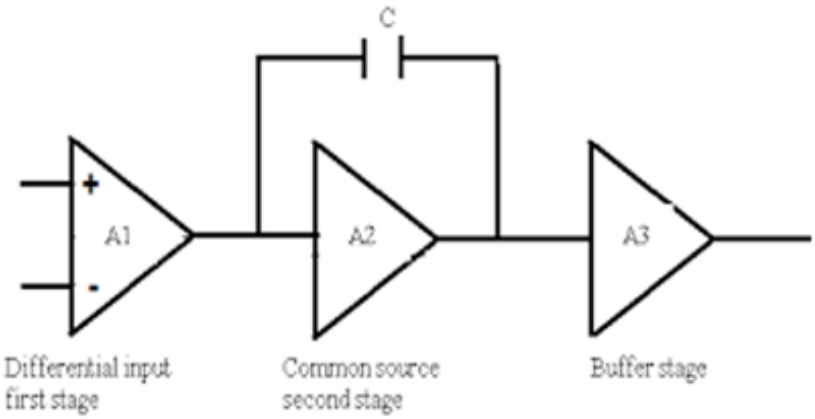

Figure 1.1: Block Diagram of a Current-Buffer Two-Stage Op-amp.

As this stage uses differential input, unbalanced output differential amplifier, so it provides the required extra gain. The bias circuit is provided to establish the proper operating point for each transistor in its saturation region. Finally, we have the output buffer stage. It provides the low output impedance and larger output current needed to drive the load of op-amp or improves the slew rate of the op-amp. Even the output stage can be dropped; many integrated applications do not need low output impedance. Moreover, the slew rate permitted by the gain stage can be sufficient for the application. If the op-amp is intended to drive a small purely capacitive load, which is the case in many switched capacitor or data conversion applications, the output buffer is not used. When the output stage is not used in the circuit, it is an operational transconductance amplifier, OTA. The purpose of the compensation circuit is to lower the gain at high frequencies and to maintain stability when negative feedback is applied to the op-amp.[10]

1.3 Three-Stage CMOS Operational Amplifier

1.3.1 Basic Principles

Three-stage op-amps add an additional gain stage to the traditional two stage structure (differential input stage + gain stage) to address design challenges under the demands of high gain, high bandwidth, and high driving capability, as shown in

Fig.1.2. Differential input stage (first stage) provides high common mode rejection ratio (CMRR) and low noise. Intermediate gain stage (second stage) provides the main voltage gain. Output buffer stage (third stage) provides low output impedance for enhanced drive capability. Differential input stage (first stage) structure: PMOS/NMOS differential pair plus active load (current mirror). Converts differential input signals to single-ended signals, provides high common mode rejection ratio, determines input noise and distortion voltage. Intermediate gain stage (second stage) Architecture Common-source amplifier (NMOS/PMOS) plus current-source load. Provides the main voltage gain and level shift, determines the gain bandwidth product of the op-amp, improves the output impedance with cascode structure, Miller compensation for stability. Output buffer stage (third stage) structure: Class-AB push-pull output stage, provides low output impedance, enhanced driving capabilities, increased swing rate, reduced crossover distortion with floating bias, feed-forward compensation for improved stability.

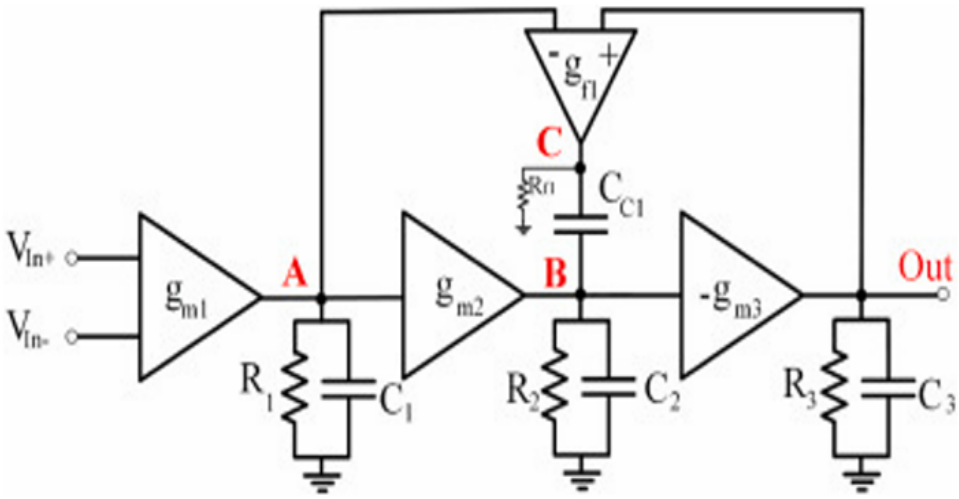

Figure 1.2: Block Diagram of a Three-Stage Op-amp.

The input stage features a rail-to-rail differential pair with active load current mirrors, providing high common-mode rejection ratio (CMRR) and low input-referred noise characteristics. The differential amplifier stage employs to enhance the overall open-loop gain while maintaining adequate phase margin, The output stage utilizes a class-AB push-pull configuration with adaptive biasing, delivering robust output

current drive capability up to 50mA with minimal crossover distortion, The bias generation circuit incorporates a band-gap reference and start-up circuitry to establish stable operating points for all amplifier stages. Advantages of three-stage op-amp: ultra-high gain (>100dB), strong driving ability, low distortion. Three-stage op-amps offer irreplaceable advantages in scenarios requiring ultra-high precision and strong drive through reasonable gain allocation and compensation strategies.

Three stage op-amps are used in applications where low power is required or that can operate with low supply voltage or with minimal power from V_{DD}. In comparison to two-stage op-amps the bias circuit to be developed can pull more current from V_{DD} than the op-amps it biases. For proper operation of the output stage floating current sources are generally preferred. To keep large gain and lowering the power supply voltage, considering the three stage op-amp is advantageous. The design is cascade of two different differential amplifier stages followed by a common source amplifier. If we connect a resistive load to the output of the common source stage, the overall op-amp gain remains relatively high due to the cascaded gain of two differential amplifier stages. This topology of op-amp i.e. more than two stages is a sort of compensation of capacitors within the op-amp for overall improvement in the desired op-amp characteristics.[10, 11]

1.4 Statements of the problem

Comparing a three-stage CMOS op-amp and a current buffer two-stage CMOS op-amp primarily revolves around addressing inherent trade-offs in performance metrics such as gain, speed (gain-bandwidth product), power consumption, and stability/compensation complexity. The core problems this research aims to address are:

- **Trade-offs in Three-Stage Amplifiers**: Conventional three-stage CMOS op-amps can achieve high DC open-loop gain, which is often a primary design goal, but this comes with significant challenges in frequency compensation. The complex compensation networks required often lead to reduced gain-bandwidth product (GBW), larger die area due to large compensation capacitors, and increased power consumption to maintain stability across varying load conditions.
- **Performance Limitations in Two-Stage Amplifiers**: Standard two-stage CMOS op-amps are generally more stable and offer better speed performance

than three-stage designs, but often struggle to achieve the very high DC open-loop gain required for some precision applications, especially in modern low-voltage, short-channel CMOS technologies where the intrinsic gain of a single transistor is lower.

- **Evaluating the Current Buffer Solution**: The current buffer technique in a two-stage op-amp is a proposed method to potentially enhance specific performance parameters, such as DC gain and voltage swing, while aiming for lower power dissipation. The problem is the lack of a clear, quantitative comparative analysis that systematically evaluates if this architecture can surpass or effectively balance the comprehensive performance of a three-stage amplifier, specifically concerning all key performance metrics (gain and voltage swing).

Therefore, the research problem is to determine the optimal architecture for modern integrated circuits by providing a comprehensive, side-by-side performance comparison to identify which topology offers a superior set of characteristics for specific application requirements, such as those in medical devices or high-speed data converters.

1.5 Research Questions

1. Performance Metrics: How do key performance parameters (DC gain, Unity Gain Bandwidth/UGB, and voltage swing) of the three-stage CMOS op-amp compare to those of the current buffer two-stage CMOS op-amp ?

2. Stability and Frequency Compensation: What are the differences in frequency compensation requirements and stability (e.g., phase margin, gain margin) between the inherently more complex three-stage architecture and the current buffer two-stage design?

3. Power and Efficiency: Which architecture offers a better trade-off between power dissipation and overall circuit performance (e.g., as measured by a Figure of Merit (FOM)) for specific low-power/high-speed applications?

4. Design Complexity and Area: How does the design complexity and physical chip area requirements for each op-amp topology compare, particularly in the context

of modern scaling CMOS technologies where vertical stacking (cascoding) is more challenging?

5. Output Drive Capability: How does the integration of a current buffer influence the two-stage op-amp's ability to drive various loads (especially capacitive loads) compared to the conventional three-stage design?

1.6 Objective of the Study

General Objective of the Study

The main objective of the study is to perform a comprehensive comparative analysis of a three-stage CMOS op-amp and a current buffer two-stage op-amp based on key performance parameters.

Specific Objective of the Study

- To design both op-amp architectures using a specific CMOS technology node and a consistent power supply.
- To simulate and extract key performance metrics: DC open-loop gain, unity gain bandwidth (UGB), phase margin, and voltage swing.
- To compare the theoretical and simulation results for both designs.
- To identify the strengths and weaknesses of each architecture.

1.7 Significance of the Study

The significance lies in the comparative analysis and evaluation of the two different op-amp configurations across two performance metrics: DC open loop gain and voltage swing.

- Performance Trade-offs: The research work investigates the critical trade-offs in analog circuit design.
- Optimization for Specific Applications: By comparing parameters like DC gain, unity gain frequency (GBW), phase margin, voltage swing, and power consumption, the research offers valuable guidance on which topology is better suited for specific needs.

- Contribution to Design Knowledge: The thesis contributes to the existing body of knowledge by offering a clear framework for analyzing and refining high-performance, stable, and versatile electronic systems, especially with the ongoing trend of incorporating analog circuits into highly integrated digital chips (mixed-signal systems).

1.8 Scope of the Study

The study involves the following key areas of Design and Simulation:

- Circuit Design: The research involves the design of both a conventional three-stage CMOS op-amp and a two-stage CMOS op-amp that incorporates a current buffer technique.
- Technology Node: The designs were implemented using CMOS technology nodes and defined power supply voltage.
- Software Tools: The design and simulation were carried out using Cadence OrCAD and Allegro SPB v17.4 to verify the circuit behavior.

Chapter 2

LITERATURE REVIEW

2.1 Operational Amplifier Overview

Operational amplifiers are an integral part of many analog and mixed signal systems. Op-amps with vastly different levels of complexity are used to realize functions ranging from DC bias generation to high speed amplification or filtering. Ideal op-amp and its parameter values, basic op-amp structure and its parameters such as DC open loop gain, gain bandwidth product, common mode rejection ratio, power supply rejection ratio etc. will be discussed. An op-amp is a differential amplifier with two inputs and one output, infinite gain, infinite input resistance and zero output resistance, as shown in Fig.2.1.

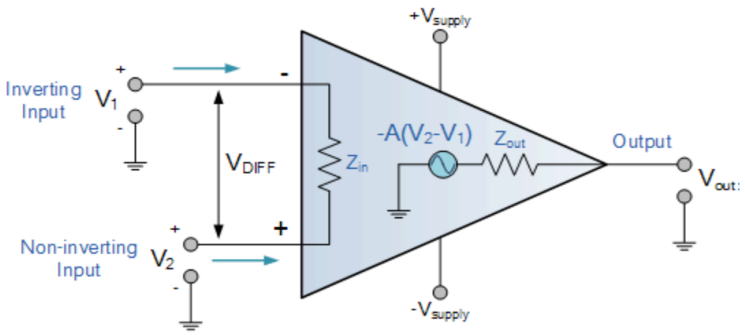

Figure 2.1: Standard Op-amp Model

The standard op-amp model is shown in Fig. 2.1 which amplifies the voltage difference, $V_D = V_P - V_N$, on the input ports and produces a voltage, V_0, on the output

port that is referenced to ground. The ideal op-amp model was derived to simplify circuit calculations and is commonly used by electronics engineers in first order approximation calculations. The ideal model makes three simplifying assumptions:

- Gain $(A_V) = \infty$
- Input Resistance $(R_{in}) = \infty$
- Output Resistance $(R_0) = 0$

Applying these assumptions to Fig. 2.1 results in the ideal op-amp model is shown in Fig. 2.2.

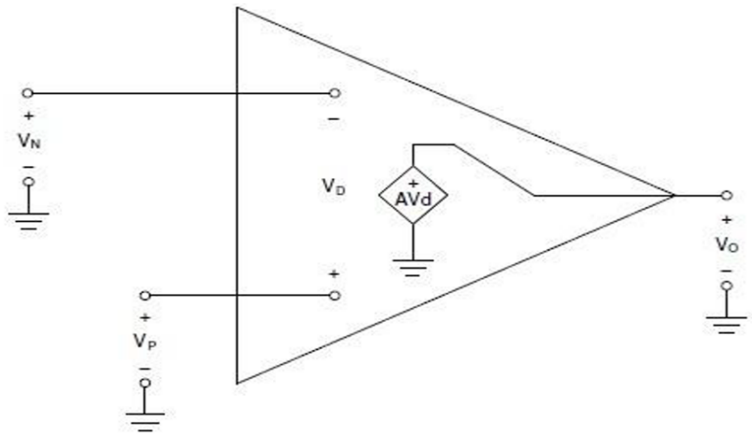

Figure 2.2: Ideal Op-Amp Model

- Since $R_{in} = \infty$, we assume $I_P = I_N = 0$
- $V_0 = A_V \times V_d$. Since $R_0 = 0$, there is no loading effect at the output. $V_d = 0$
- Output Resistance $(R_0) = 0$

If the op-amp is in linear operation, V_0 must be a finite voltage. By definition, $V_0 = A_V \times V_d$. On rearranging, $V_d = V_d/A_V$. Since, $A_V = \infty$, $V_d = 0$. This is the basis for the virtual short concept.

- Common mode gain = 0.
  The ideal voltage source driving the output port depends only on the voltage difference across its input port. It rejects any voltage common to V_N and V_P.
- Bandwidth = ∞.
- Slew Rate = ∞.
- No frequency dependencies are assumed.
- Drift = 0

There are no changes in performance over time, temperature, humidity, power supply variations, etc.

2.2 Stages Of CMOS Op-Amps

Operational amplifiers (Op-Amps) are principal element in an analog system. System stability is fundamental in various research areas such as voltage stability employing voltage regulators and capacitors.[12, 13] Op-amps have been used in power management ICs, data converters, filters, sensors, regulators etc. Most of these applications are made by employing op-amp circuits in negative feedback, which also helps to achieve stability. With the continued scaling in technology node, transition frequency is high and results in faster transistors. But the transconductance, output resistance and hence the intrinsic gain ($g_m \times r_0$) of transistor is decreased. With scaling in supply voltage, low-power circuits should reduce thermal dissipation with the trend in miniaturization.[14] As a result, gain of the analog systems decreases consistently with the scaling. One obvious solution is cascoding, which is a vertical stacking of devices.

The problem with stacking is that there will be a swing limit and is not suited for low voltage design.[15] In order to overcome this, we must go with horizontal cascading. The process variations become significant with scaling leading to random offsets.[16, 17] Scaling also affects the linearity and accuracy of analog systems. The DC gain of individual stages must be increased to compensate the effect of scaling on accuracy. Thus, to meet the gain requirements of op-amp at nano-scale process, multi-stage op-amp topologies have become important.[18] However, the multistage op-amp suffers

from the closed loop stability and bandwidth reduction due to increasing the number of frequency poles.[19] We can use a "high-gain differential amplifier;" by high we mean a value that is adequate for the application, typically in the range of 10^1 to 10^5. Since op-amps are usually employed to implement feedback system, their open loop gain is chosen according to the precision required of the closed loop circuit.

2.3 Current Buffer Two-Stage CMOS Op - Amp

Operational amplifiers are one of the basic and important circuits which have a wide application in several analog circuits such as switched capacitor filters, algorithmic, pipelined and sigma delta A/D converter, sample and hold amplifier etc. The speed and accuracy of these circuits depend on the bandwidth and DC gain of the operational amplifiers. Operational amplifiers with larger bandwidth and gain, higher speed and accuracy are a critical element in analog sampled data circuit, such as SC filters and modulators.[20] The current buffer two-stage op-amp is shown in Fig.2.3. The first block is a differential amplifier, which has two inputs: the inverting and non-inverting inputs. The differential amplifier provides, at the output, a differential voltage or a differential current that depends on the differential inputs only.

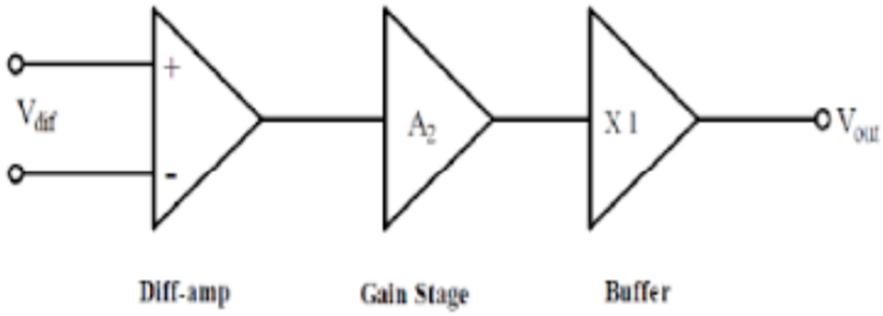

Figure 2.3: A Current Buffer Two-Stage Op-Amp Model.

The second block is a differential to single-ended converter. It is used to transform the differential signal generated by the first block into a single ended version. Some architecture doesn't require the differential to single ended function; therefore, the second block can be excluded. In most cases the gain provided by the input stages is

not sufficient and additional amplification is required. This is provided by an intermediate stage, which is another differential amplifier, driven by the output of the first stage. As this stage uses differential input-unbalanced output differential amplifier, so it requires extra gain. The bias circuit is provided to establish the proper operating point for each transistor in its saturation region. Finally, we have the output buffer stage. It provides the low output impedance and larger output current needed to drive the load of operational amplifier or improves the slew rate of the operational amplifier. Even the output stage can be dropped; many integrated applications do not need low output impedance. Moreover, the slew rate permitted by the gain stage can be sufficient for the application. If the operational amplifier is intended to drive a small purely capacitive load, which is the case in many switched capacitor or data conversion applications, the output buffer is not used. When the output stage is not used in the circuit, it is an operational transconductance amplifier (OTA). The purpose of the compensation circuit is to lower the gain at high frequencies and to maintain stability when negative feedback is applied to the operational amplifier.[21]

A classic op-amp architecture is made up of three, even though it is referred to as a "two-stage" op-amp, ignoring the buffer stage (the third stage). The first stage has the most dominant pole of the system. A common source amplifier usually meets the specification of second stage, having a moderate gain. The third stage is most commonly implemented as a unity gain source follower with a high frequency and negligible pole.[22] With the two stage classic op-amp architecture, high gain stages are difficult to achieve with Complementary Metal Oxide Semiconductor (CMOS) technology and basic amplifier topologies. A typical CMOS differential amplifier stage is shown in Fig.2.4. The input devices in Fig. 2.4 are p-channel MOSFETs (PMOS). PMOS input devices are used more because of improved slew rate and reduced 1/f noise.[22] PMOS input devices also provides reduced power supply rejection ratio due to the current mirror's low sensitivity to change in power supply voltage.

For the CMOS differential input stage, the gain and bandwidth are calculated respectively as follows:

$$A_1 = g_{m1} \times (r_{ds2} || r_{ds4}) \tag{2.3.1}$$

and

$$\omega_1 = \frac{1}{C_{out}} \times (r_{ds2} || r_{ds4}) \tag{2.3.2}$$

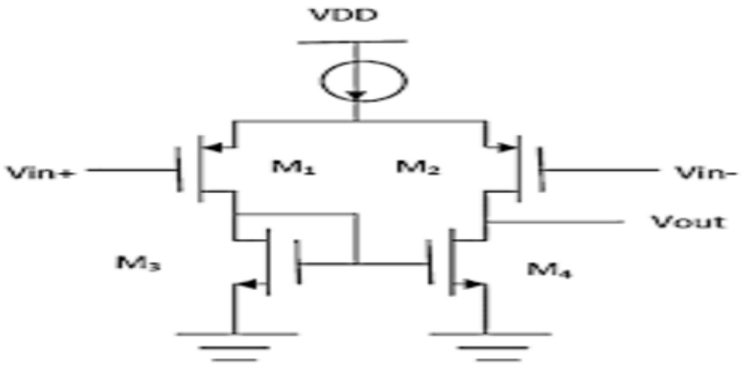

Figure 2.4: CMOS Differential Input Stage.

Implementation of cascade scheme can increase the moderate gain of this stage to a high value. The stage's dominant pole has an output capacitance, C_{out}, consisting of mainly, the drain-to-bulk capacitance of M_2 and M_4. Although often negligible, another pole and zero are generated by M_1 and M_3.[23]

The second stage implementation of a common source amplifier is shown in Fig. 2.5.

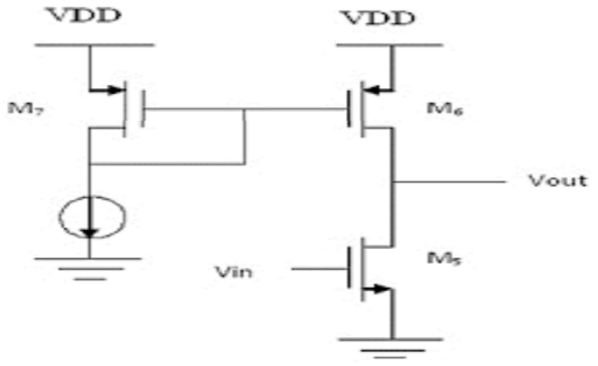

Figure 2.5: Common Source Amplifier Stage.

Similar to the first stage, additional cascade devices can increase the gain of this stage. Higher gains are often desirable for this stage when using Miller compensation

techniques, although higher gains leads to lower bandwidth and the designer has to decide between these trade-offs based on the specifications of the system. For the circuit in Fig. 2.5, the gain and bandwidth are calculated respectively as follows:

$$A_2 = g_{m5} \times (r_{ds5} || r_{ds6}) \tag{2.3.3}$$

and

$$\omega_2 = \frac{1}{C_{out}} \times (r_{ds5} || r_{ds6}) \tag{2.3.4}$$

The output capacitance is dominated by the drain-to-bulk capacitance of M_5 and M_6. The final output stage is normally realized with a simple source follower. With gain less than, but closer to unity, the source follower acts as a buffer for the previous two stages, reducing the overall gain negligibly and barely affecting the overall bandwidth with its high frequency pole. The gain for the source follower is defined as:

$$A_3 = \frac{g_{m8}}{(G_L + g_{m8} + g_{ds8} + g_{ds9})} \tag{2.3.5}$$

where, G_L is the load conductance that the stage will drive.

2.4 Three-Stage CMOS Op - Amp

Three stage operational amplifier, shown in Fig.2.6, is used in applications where low power is required or that can operate with low supply voltage or with minimal power from V_{DD}.

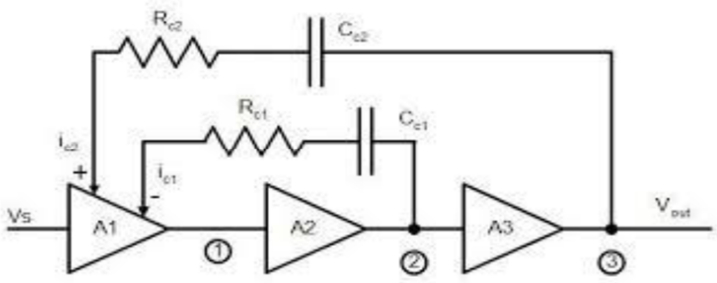

Figure 2.6: Block Diagram of Three Stage Op-Amp.

In comparison to the two-stage operational amplifiers, the bias circuit to be developed can pull more current from V_{DD} than the operational amplifiers it biases. So, we have used two circuit architectures for biasing circuits. For proper operation of the output stage, floating current sources are generally preferred. In order to produce a large gain and lower the power supply voltage, the three stage operational amplifier is the most preferred design. The design is cascade of two different differential amplifier stages followed by a common source amplifier. If we connect a resistive load to the output of the common source stage, the overall operational amplifier gain remains relatively high due to the cascaded gain of two differential amplifier stages. This multi-stage topology requires advanced compensation. Nested Miller Compensation (NMC) or Reversed-NMC (RNMC) eliminates stability issues from multiple poles.[24]

2.5 Op - Amp Performance Parameters

DC Open Loop Gain:
Open loop gain is ratio of the change in output DC voltage to the change in DC input voltage gain. An ideal op-amp has infinite DC open-loop gain. Very high gain of the op-amp enables considerable levels of feedback to be applied to achieve the required performance.

$$A_0 = A_1 A_2 A_3 ... A_n \tag{2.5.1}$$

where, A_0 is overall DC open loop gain of the amplifier, A_1, A_2, A_3, ..., A_n are the gains of the first stage, second stage, third stage and n^{th} stage, respectively. The open loop gain of practical op-amp is constant only at low frequency and it falls rapidly with increasing frequency, as shown in Fig.2.7.

2.5.1 Gain Bandwidth Product (GBW)

Gain bandwidth product can be described as the product of the open loop gain and the frequency of the dominant pole. It is also known as the unity gain frequency or the frequency at which the gain of the operational amplifiers are unity (0 dB), as shown in Fig.2.7.[25]

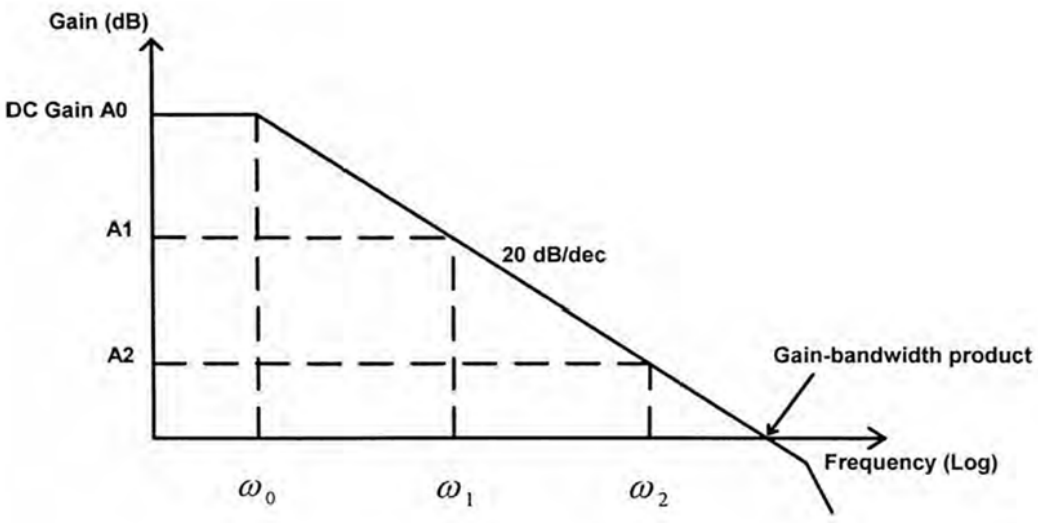

Figure 2.7: DC Open Loop Gain of a Typical Op-Amp.[25]

It is given by:

$$GBW = A_V \times \omega \tag{2.5.2}$$

Gain bandwidth product is constant for a given operational amplifier. The frequency response of an operational amplifier circuit depends only upon the gain bandwidth product and not upon the gain and the bandwidth individually.

$$A_0 \times \omega_0 = A_1 \times \omega_1 = A_2 \times \omega_2 = ... \tag{2.5.3}$$

Hence, there is a trade-off between gain and bandwidth for a given operational amplifier design such as high gain at a lower frequency or lower gain at a higher frequency. Cut - off frequency (ω_0): is the frequency where the gain of the operational amplifier is reduced by a 3dB.

2.5.2 Phase Margin

Phase margin is defined as the difference between the actual phase of the loop gain and -180^0, measured at the frequency where the loop gain magnitude is exactly 0dB (unity gain). Phase margins is a measure of how close an amplifier is to become unstable and oscillating. A typical phase margin is greater than 60^0; a lower phase margin (like 45^0 or less) will cause ringing.[25, 26]

The following are some typical previous research results on DC open loop gain, GBW and PM. J. Mahattanakull achieved a DC open loop gain of 78.21378dB, -3dB cut-off frequency of 771.63Hz, PM of 63.97^o, and GBW (UGB) of 5.82MHz for L=0.35μm, as shown in Fig.2.8.[27]

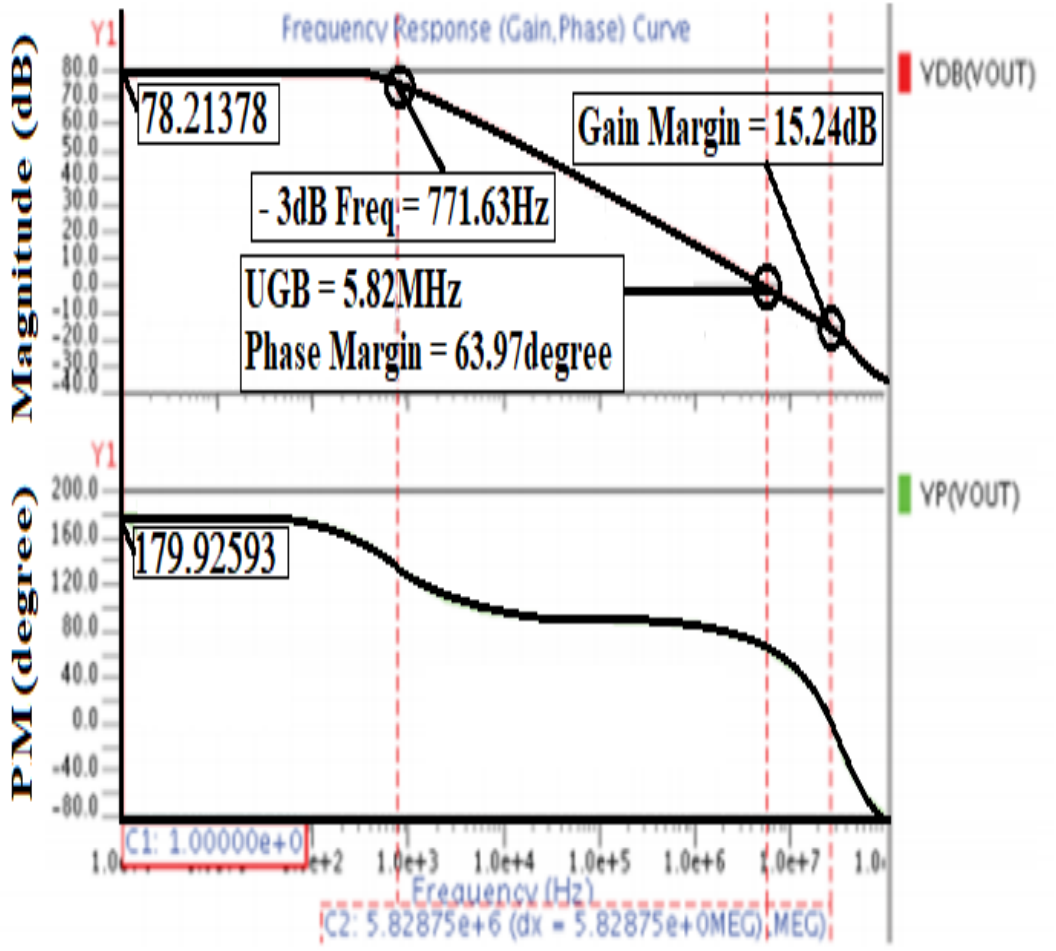

Figure 2.8: Experimental Simulation Result of Gain and PM by J. Mahattanakull.[27]

K. T. Tan, et. al., obtained an open loop gain of 21.18dB, GBW (UGB) of 6.31MHz, and PM of 94.26^0, on a 0.18μm CMOS technology, with a supply voltage of $\pm$1.8V, as shown in Fig.2.9.[28]

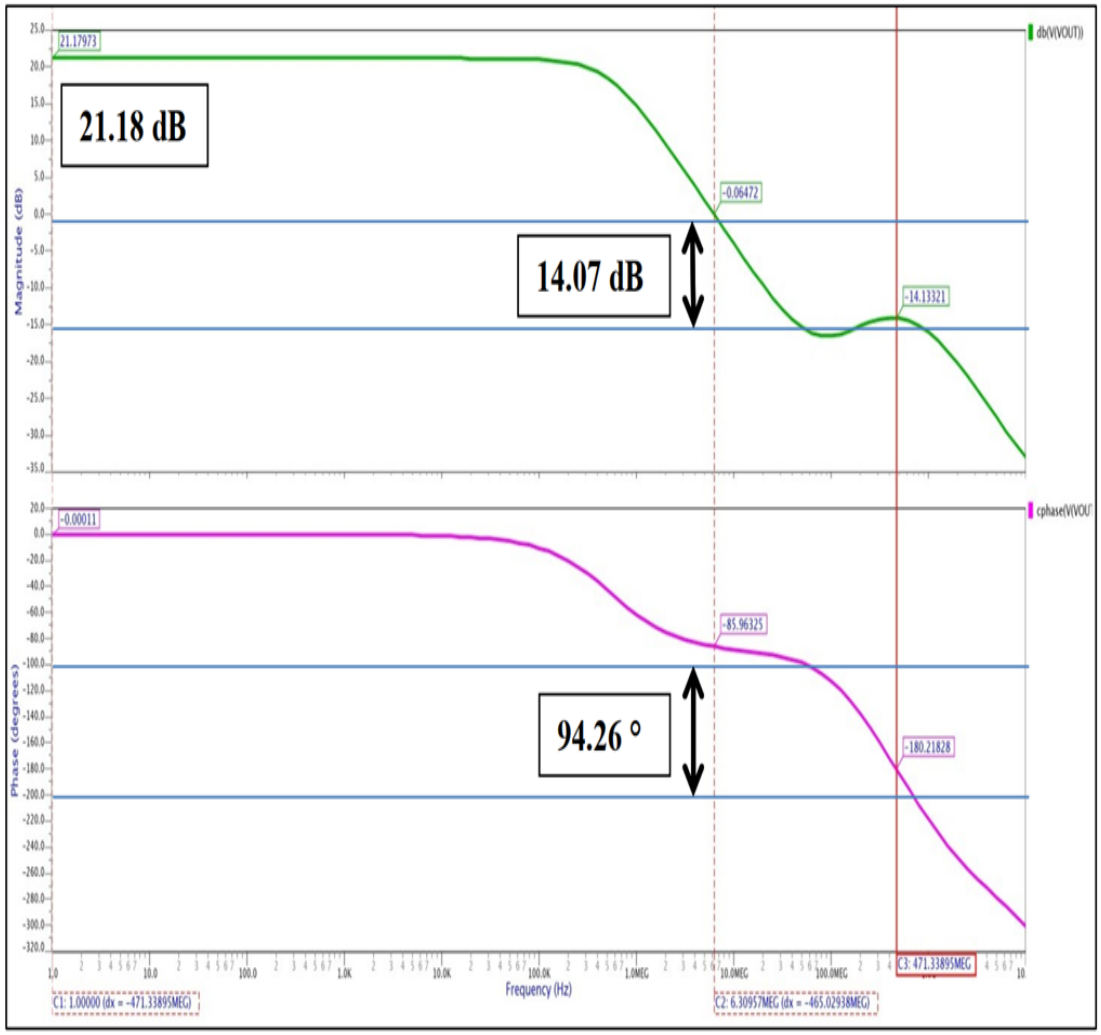

Figure 2.9: Simulation result of open loop gain done by K. T.Tan, et. al.[28]

Likewise, Abolfazl Sadeqi, et. al. provided simulation result of an open loop gain of 79.5dB, GBW (UGB) of 5.9MHz and PM of 62^0 in HSPICE, as shown in Fig.2.10.[29]

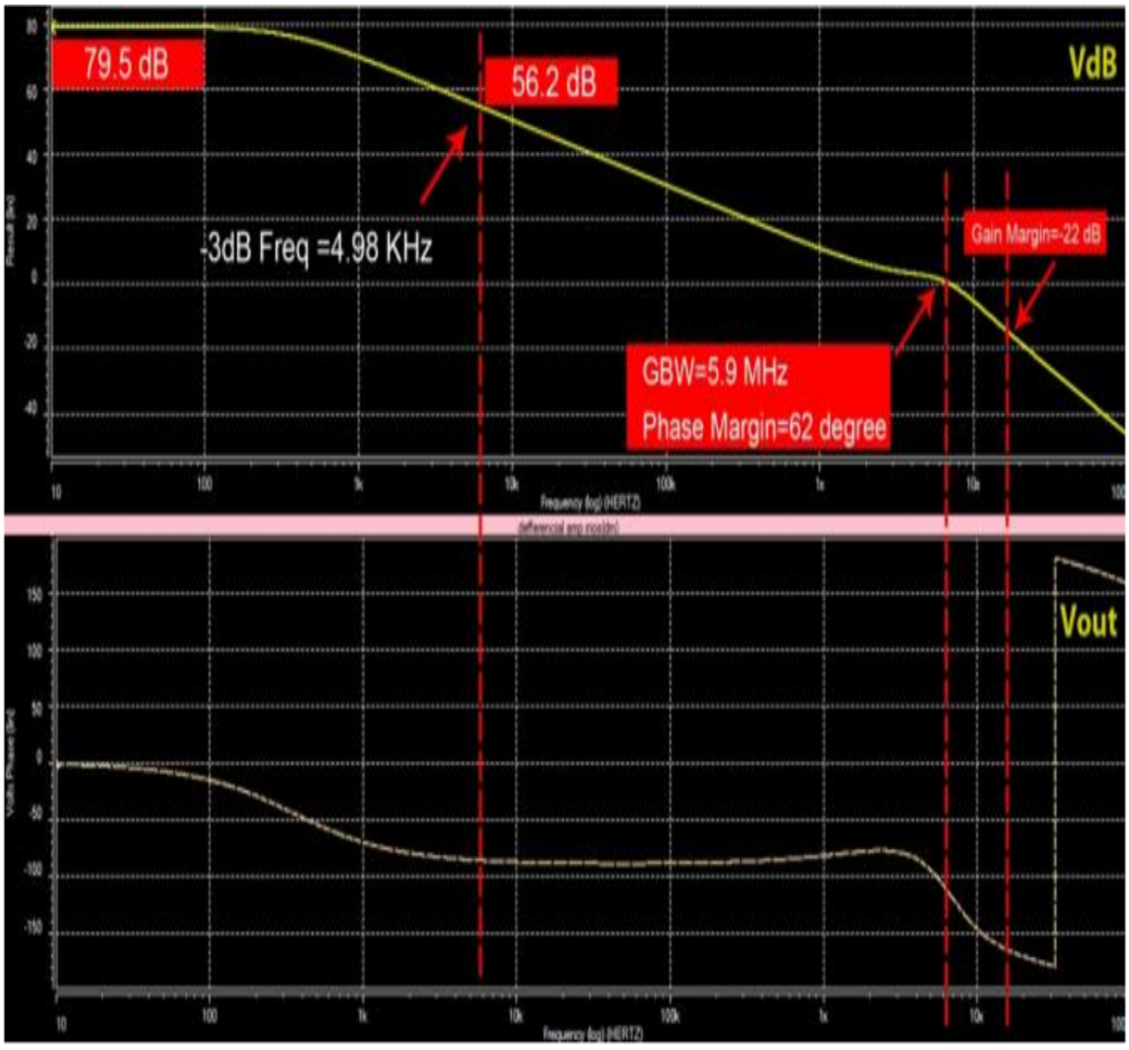

Figure 2.10: Simulation result of open loop gain done by Abolfazl Sadeqi, et. al.[29]

An open loop gain of 107dB, GBW of 57.48MHz and PM of 64.83^0 based on SMIC 0.18μm CMOS process model, with a supply voltage of $\pm$1.8V, has been obtained by H. Qiao, as shown in Fig.2.11.[30]

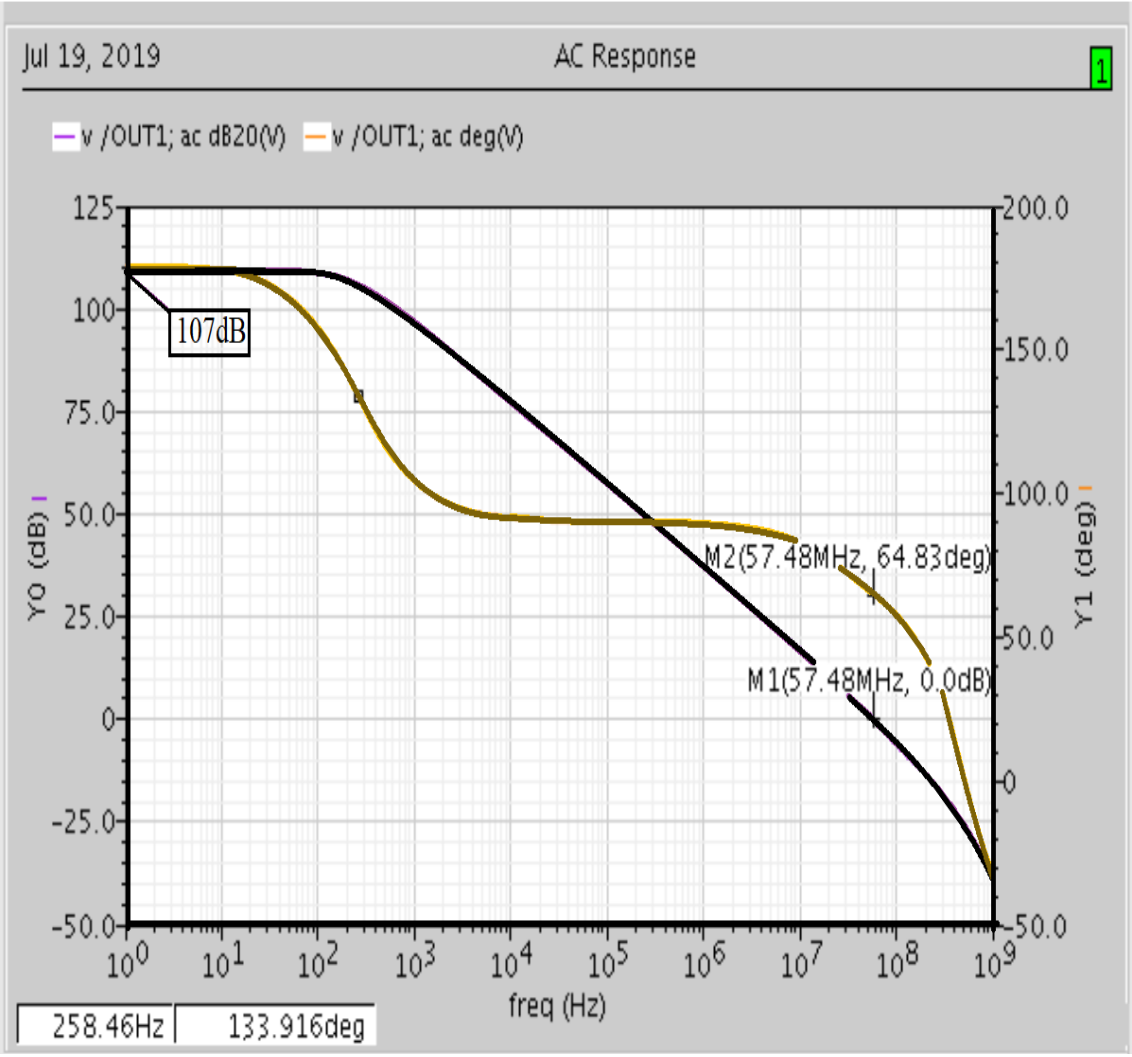

Figure 2.11: Simulation result of open loop gain done by H. Qiao.[30]

L. Tianwang, et al., obtained an open loop gain of 59dB, GBW (UGB) of 282MHz, and PM of 66^0 on a 0.18μm CMOS technology, with a supply voltage of $\pm$1.8V, as shown in Fig.2.12.[31]

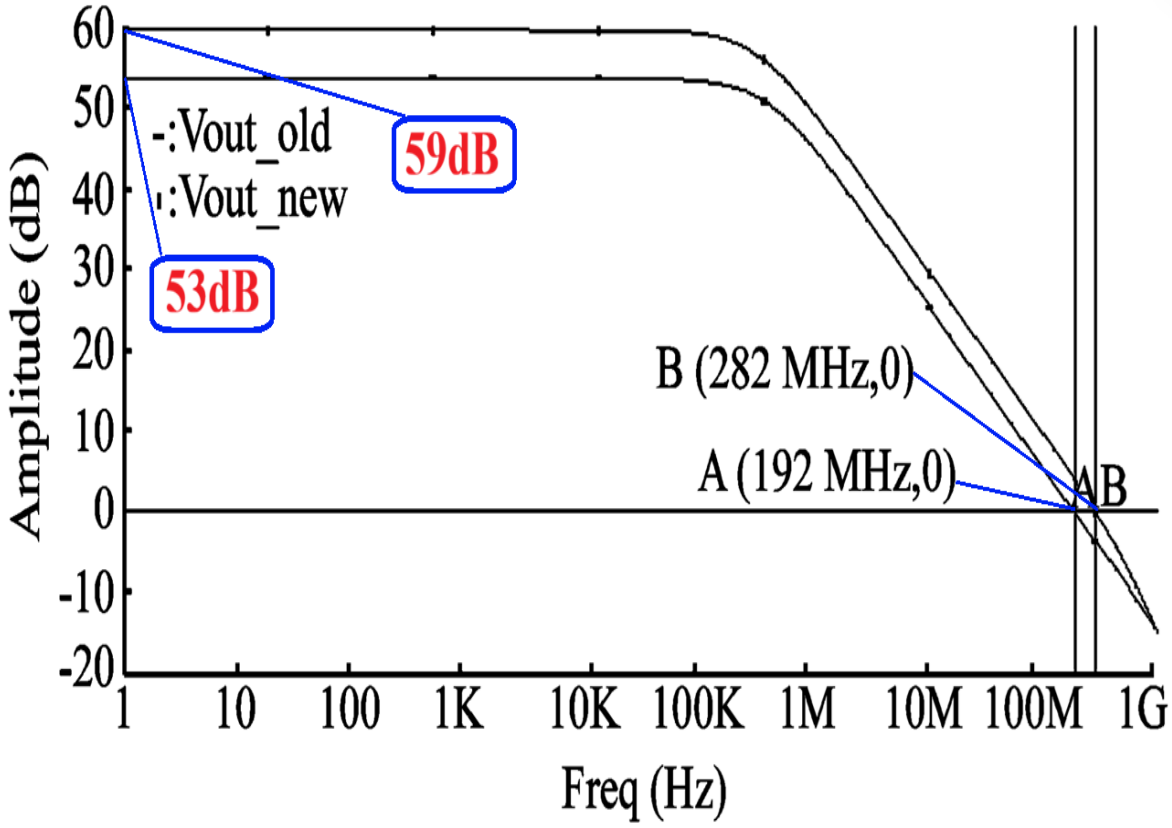

Figure 2.12: Simulation result of open loop gain done by L. Tianwang, et. al.[31]

Fig.2.13 shows the simulation result for DC gain of 110.7dB, GBW (UGB) of 15.29MHz and PM of 59.89^0 with 0.8μm technology and $\pm$3V supply voltages obtained by Rien Beal.[32]

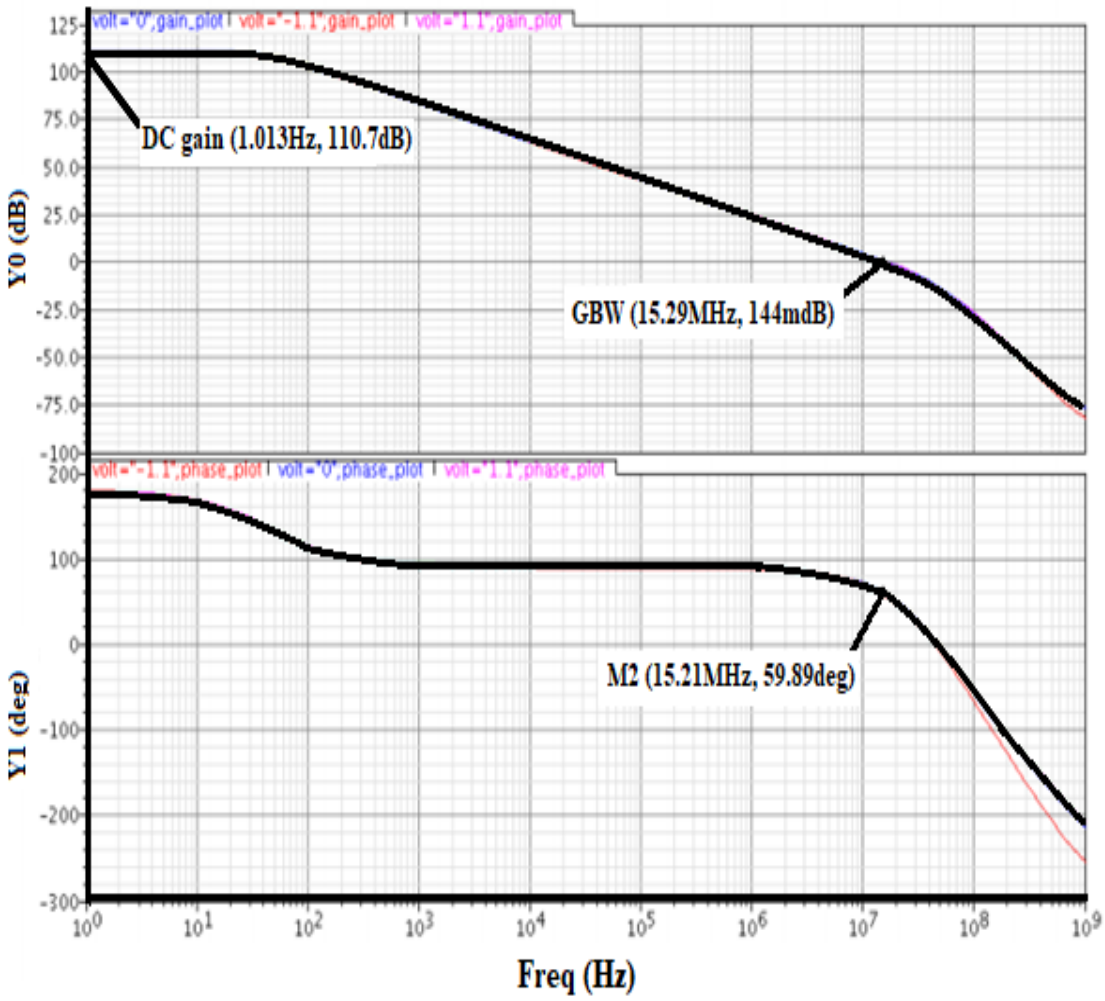

Figure 2.13: Simulation Result of Gain and Phase Response by Rien Beal.[32]

The design by Lokesh Kumar Srivastav provided a gain of 95.7dB, GBW (UGB) of 8.38MHz and PM of 55.57^0 with 0.35μm CMOS technology and 3.3V supply voltage, as shown in Fig.2.14.[33]

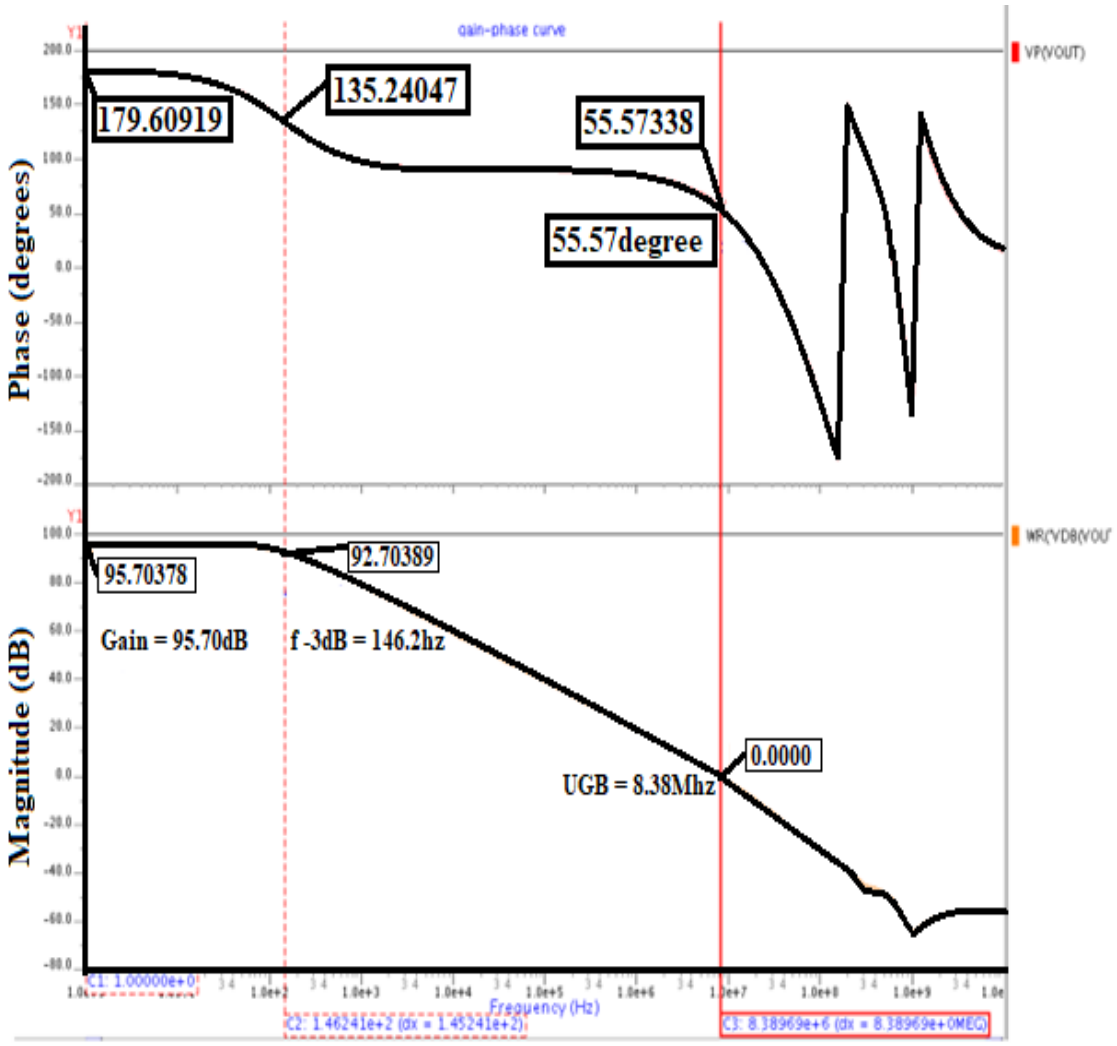

Figure 2.14: Simulation Results of Gain and PM by Lokesh Kumar Srivastav.[33]

Shahid Khan, et. al., obtained an open loop gain of 55.5dB, GBW (UGB) of 12.6MHz, and PM of 60^0 with the help of OrCAD PSPICE software by using $\pm$1.8V input voltage using TSMC 0.18μm technology, as shown in Fig.2.15.[34]

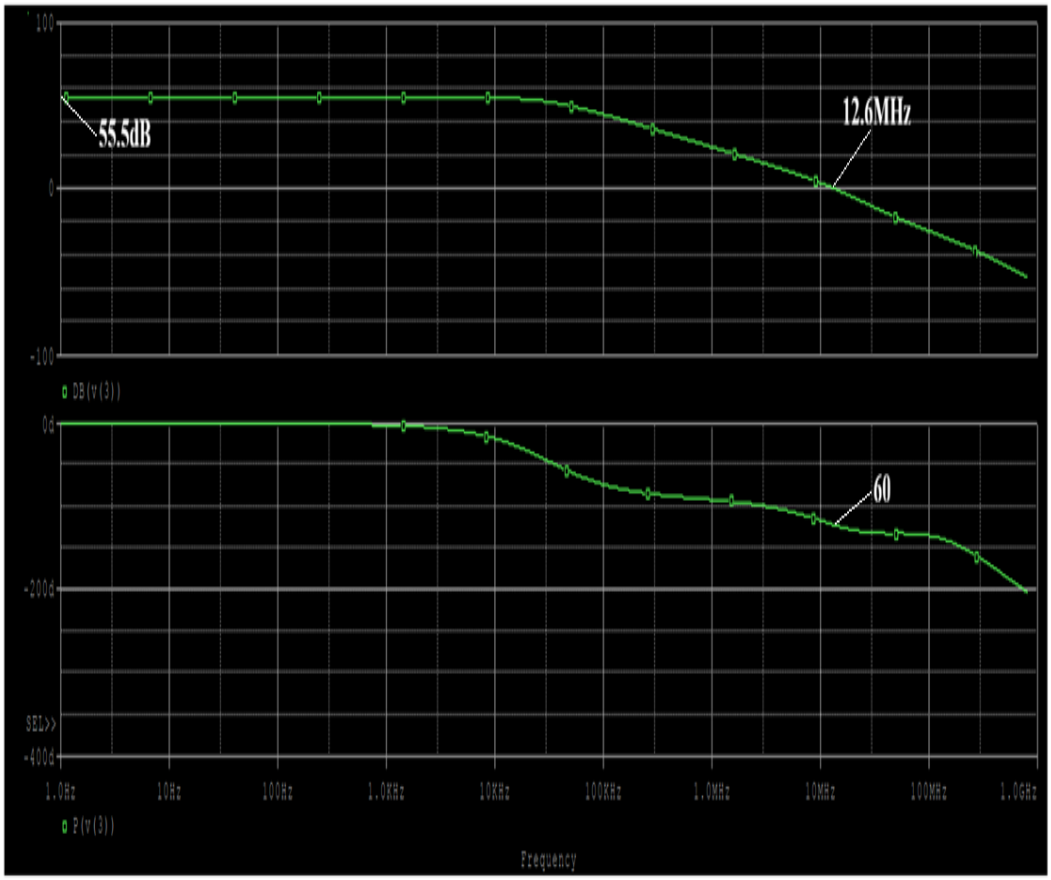

Figure 2.15: Simulation Results of Gain, GBW, and PM by Shahid Khan, et. al.[34].

A linear symbolic model was used by Rezaei, I. et al., to predict amplifier behavior while 0.18μm CMOS technology is exploited for circuit simulation. The proposed amplifier was able to achieve 115 dB DC gain, 151 MHz GBW, and 55^0 PM for a three-stage CMOS op-amp, shown in Fig.2.16.[35] N. Desai and R. Harjani found an open loop gain of 42dB and PM of 92.1^0.[36]

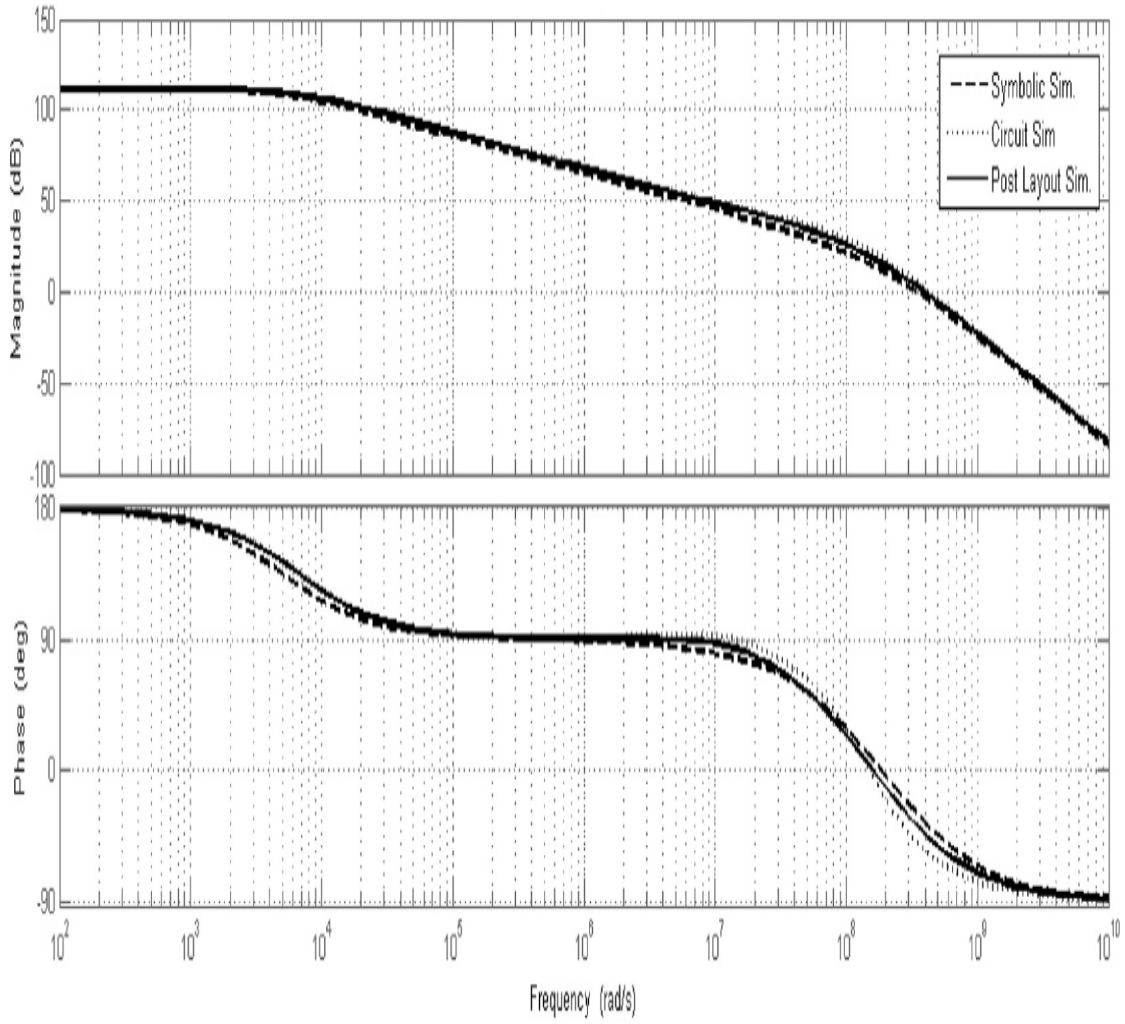

Figure 2.16: Simulation result of open loop gain done by Rezaei, I. et al.[35]

2.5.3 Output Voltage Swing

The output voltage swing is the maximum change in output voltage, measured with respect to a reference potential. Simulation results of voltage swing obtained by previous researchers are given below.

Fig.2.17 shows the simulation result of input/output voltage swing obtained byAbolfazl Sadeqi, et. al.[29]

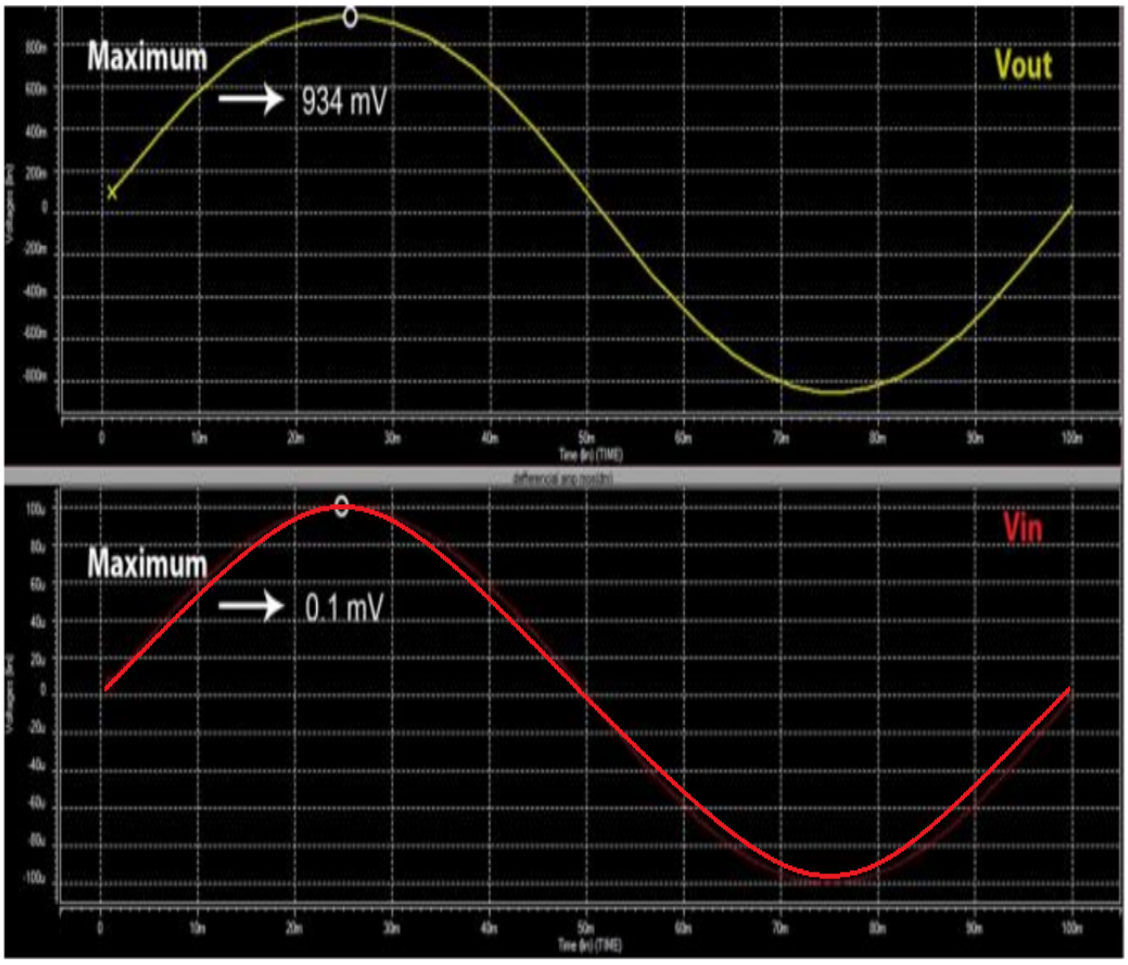

Figure 2.17: Input/Output Voltage Swing Obtained by Abolfazl Sadeqi, et. al. [29]

From Fig.2.17, the gain obtained by Abolfazl Sadeqii, et. al.[29] can be calculated as follows:

$$Gain = \frac{V_{(out,\ peak\ to\ peak)}}{V_{(in,\ peak\ to\ peak)}} = \frac{1,868mV}{0.2mV} = 9,340$$

$$Gain\ (in\ dB) = 20\log(9,340) = 79.4dB$$

The simulation result of input/output voltage swing obtained by K. S. Kumar, et al., is shown in Fig.2.18[37].

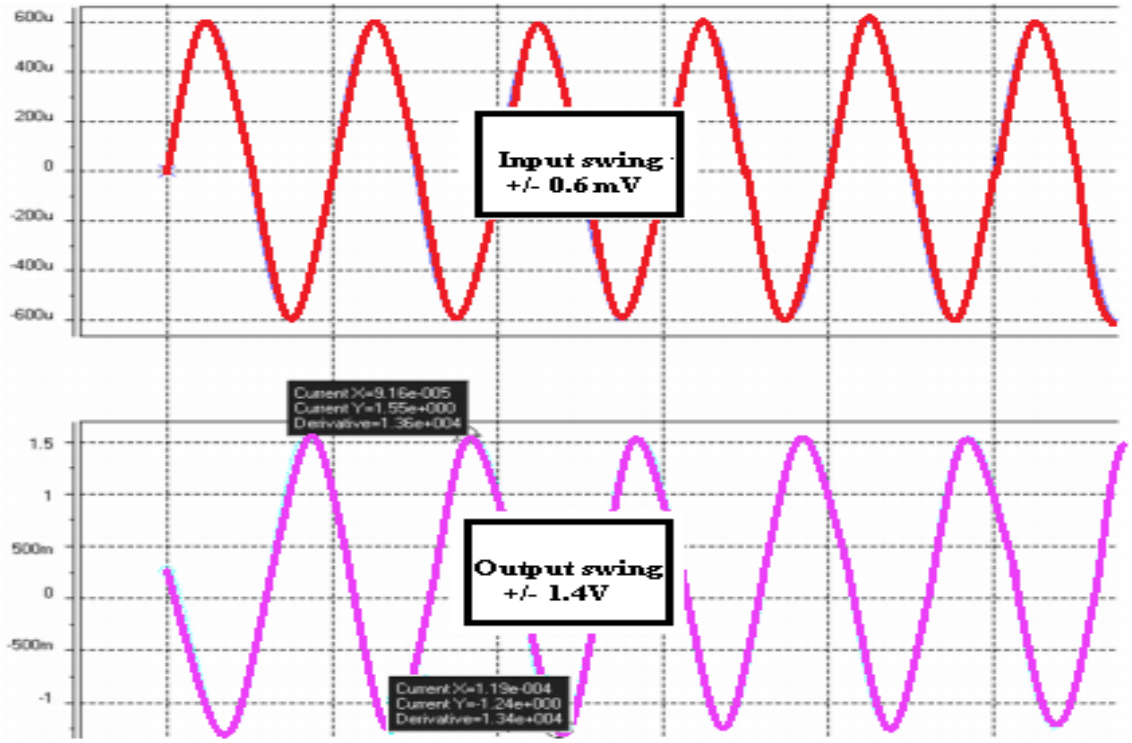

Figure 2.18: Input/Output Voltage Swing Obtained by K. S. Kumar, et al[37].

From Fig.2.18, the gain obtained by K. S. Kumar, et. al., can be calculated as follows:

$$Gain = \frac{2.8V}{1.2mV} = 2,333.33$$

$$Gain\ (in\ dB) = 20\log(2,333.33) = 67.36dB$$

Fig.2.19 shows the simulation result of input/output voltage swing obtained by H. Qiao.[30]

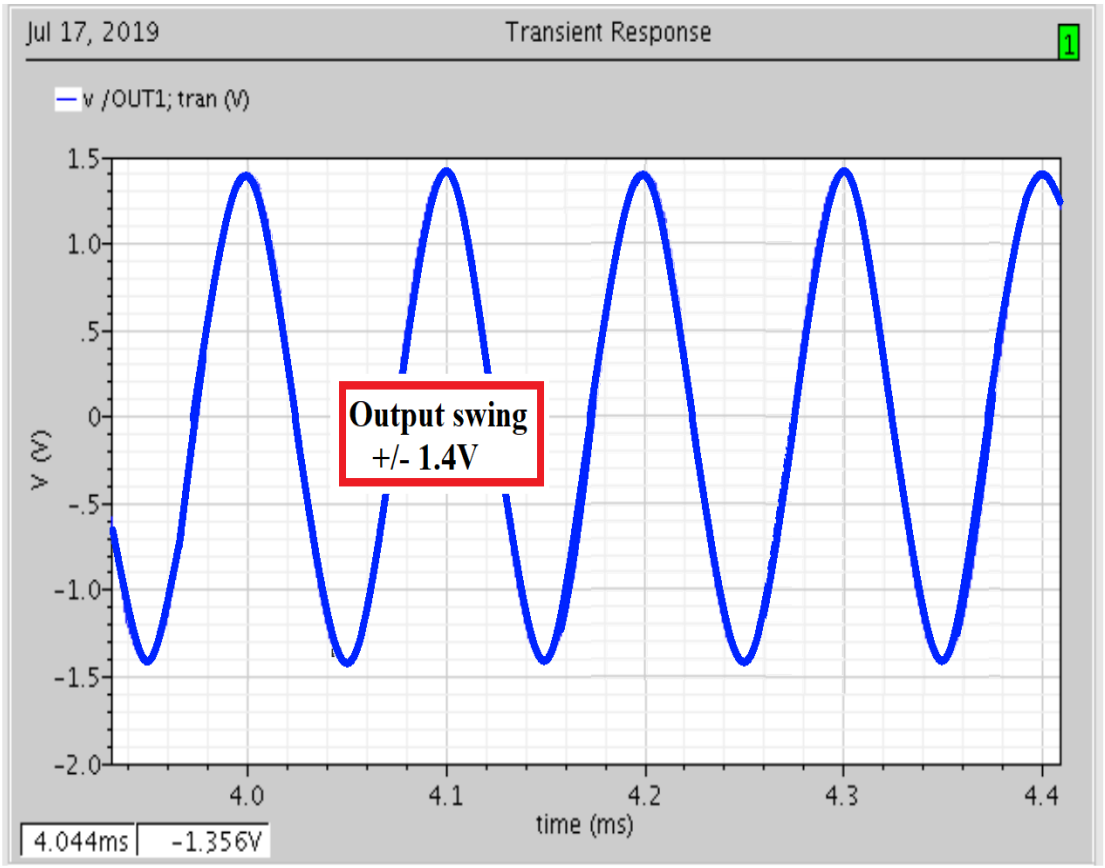

Figure 2.19: Input/Output Voltage Swing Obtained by H. Qiao,[30]

Chapter 3

METHODOLOGY

3.1 Design Topology

The following steps were used for the research's comparative analysis of a three stage CMOS operational amplifier and a current buffer two stage CMOS operational amplifier design methodology. These are specifications, circuit layout, design, simulation, analysis, and modification. The design and the optimization of the designs are two separate steps in the design process. By recommending the topology that complies with the requirements, the design's conceptualization was realized. To preserve the intuitive perspective necessary for the decisions that must be made, this stage is typically completed using hand computations. The second phase in design optimization is to take the initial draft and improve it.

The proposed methodology employs Cadence OrCAD and Allegro SPB v17.4 simulations to evaluate the performance of both the three-stage CMOS operational amplifier and the current buffer two-stage CMOS operational amplifier, incorporating considerations for environmental and process variations to enhance robustness and realism. Following this, the CMOS op-amp circuits were simulated and analyzed comprehensively. The complete schematic designs for each topology was implemented using Cadence OrCAD and Allegro SPB v17.4 software. Bias point analysis was conducted to determine the transistor drain currents. Subsequently, key device parameters such as gate-source voltage (V_{GS}), transconductance (g_m), and output conductance (g_{ds}) were derived from these drain current values. The operational amplifier parameters?including offset voltage, DC open-loop gain, output voltage swing, input common-mode range (ICMR), and power dissipation was then assessed through

simulations, supplemented by analytical calculations drawn from the reviewed literature. Finally, the CMOS op-amp parameters were iteratively adjusted as necessary to achieve optimal alignment between the simulation outcomes and the theoretical manual computations, facilitating a rigorous comparative evaluation of the two architectures.

3.1.1 Proposed Two-Stage CMOS Op-Amp with a Current-Buffer Topology

The schematic diagram of the two-stage CMOS op-amp with current buffer circuit proposed for the comparative study is shown in Fig.3.1.

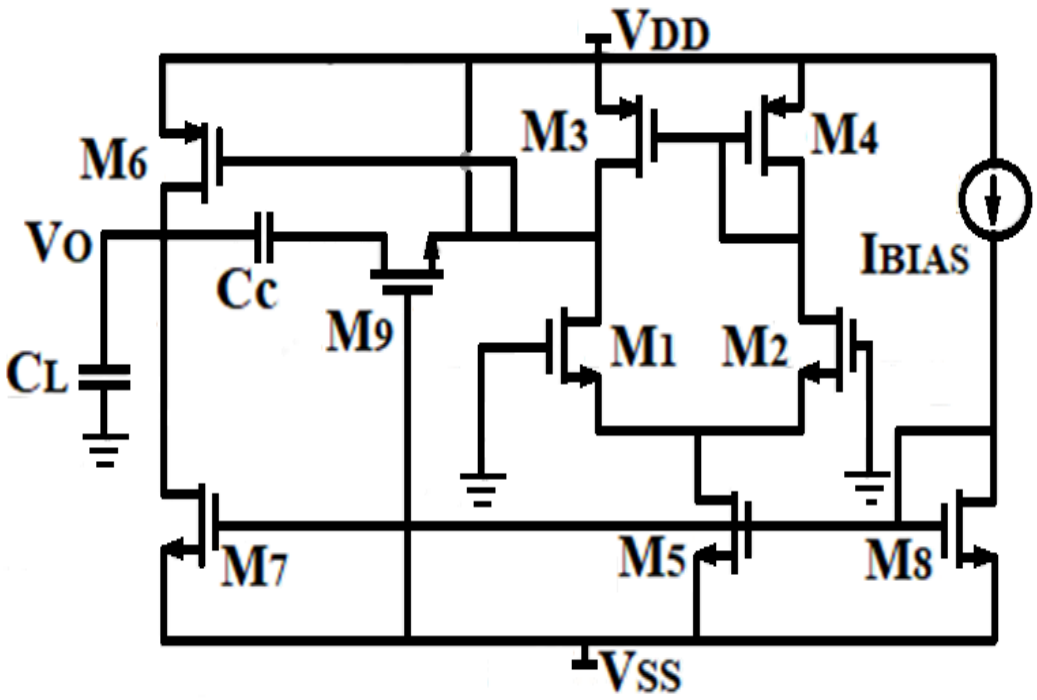

Figure 3.1: Schematic Diagram of a Current-Buffer Two-Stage CMOS Op-Amp.

Table 3.1: Table of Specifications Two-Stage CMOS Op-Amp.

S.No.	Parameters	Proposed value
1	Technology	$0.25\mu m$
2	Power supply	$\pm 3.5V$
3	Open Loop Gain	$\geq 80dB$
4	Unity Gain Bandwidth	$\geq 2.305MHz$
5	Slew Rate	$\pm 2.5\frac{V}{\mu s}$
6	Phase Marigin	$\geq 60^{\circ}$
7	Load Capacitance	10pF
8	Power Dissipation	<10mW
9	CMRR	$\geq 70dB$
10	ICMR	-2.721187V to 3.1567V

3.1.2 Design Specifications for Two-Stage CMOS Op-Amp with a Current-Buffer Topology

The specifications that are shown in Table 3.1 were used to design a two-stage op-amp. This table was used as a standard performance to evaluate different compensation techniques like a current -Buffer compensation techniques.

DC open loop Gain (A_V)**:**
The gain of the first stage is given by:

$$A_{V1} = \frac{g_{m1}}{g_{ds1} + g_{ds4}} = \frac{2g_{m1}}{I_{D5}(\lambda_2 + \lambda_4)} \tag{3.1.1}$$

The gain of the second stage is given by:

$$A_{V2} = \frac{g_{m6}}{g_{ds6} + g_{ds7}} = \frac{g_{m6}}{I_{D6}(\lambda_6 + \lambda_7)} \tag{3.1.2}$$

The overall gain A_V of the amplifier is:

$$A_V = A_{V1} \times A_{V2} = \frac{2g_{m1}g_{m6}}{I_{D5}I_{D6}(\lambda_2 + \lambda_4)(\lambda_6 + \lambda_7)} \tag{3.1.3}$$

SR:

$$SR = \frac{dQ}{C_C \times dt} = \frac{I_{D5}}{C_C} \tag{3.1.4}$$

where I_{D5} is the current through the drain of M_5 and it is also the bias current of the input stage, which will split equally between M_1 and M_2, that is, $I_{D1} = I_{D2} = \frac{I_{D5}}{2}$, if the inputs of the first stage are grounded and perfectly matched.

UGB:

$$UGB = \frac{g_{mn}}{2\pi C_C} \tag{3.1.5}$$

The transconductance of the first stage (g_{m1}) is given by:

$$g_{m1} = \sqrt{2I_D K_n \left(\frac{W}{L}\right)_1} \tag{3.1.6}$$

And the aspect ratio of M_1, $\left(\frac{W}{L}\right)_1$, is given by :

$$\left(\frac{W}{L}\right)_1 = \frac{g^2 m_1}{2I_{D1}K_n} \tag{3.1.7}$$

ICMR:

$$ICMR_{min} = (V_{GS5} - V_{TH5}) + (V_{GS1} + V_{SS}) \tag{3.1.8}$$

$$ICMR_{max} = [V_{DD} - (V_{GS4} - V_{TH4})] \tag{3.1.9}$$

Output voltage swing :

$$V_{out}^{+} = |V_{D,SAT6}| = \sqrt{\frac{2I_{D6}}{K_n \left(\frac{W}{L}\right)_6}} \tag{3.1.10}$$

$$V_{out}^{-} = |V_{D,SAT7}| = \sqrt{\frac{2I_{D7}}{K_p \left(\frac{W}{L}\right)_7}} \tag{3.1.11}$$

Power Dissipation (PD):

PD is the product of current in all the amplifier branches and the supply voltage defined in this specification. It is given by:

$$P_D = (I_{D5} + I_{D6} + I_{D8})(V_{DD} + |V_{SS}|) \tag{3.1.12}$$

$$P_D = (2I_{D5} + I_{D6})(V_{DD} + |V_{SS}|) \tag{3.1.13}$$

3.1.3 Proposed Three-Stage CMOS Op-Amp Topology

The schematic diagram of the three-stage CMOS op-amp proposed for the comparative study is shown in Fig.3.2.

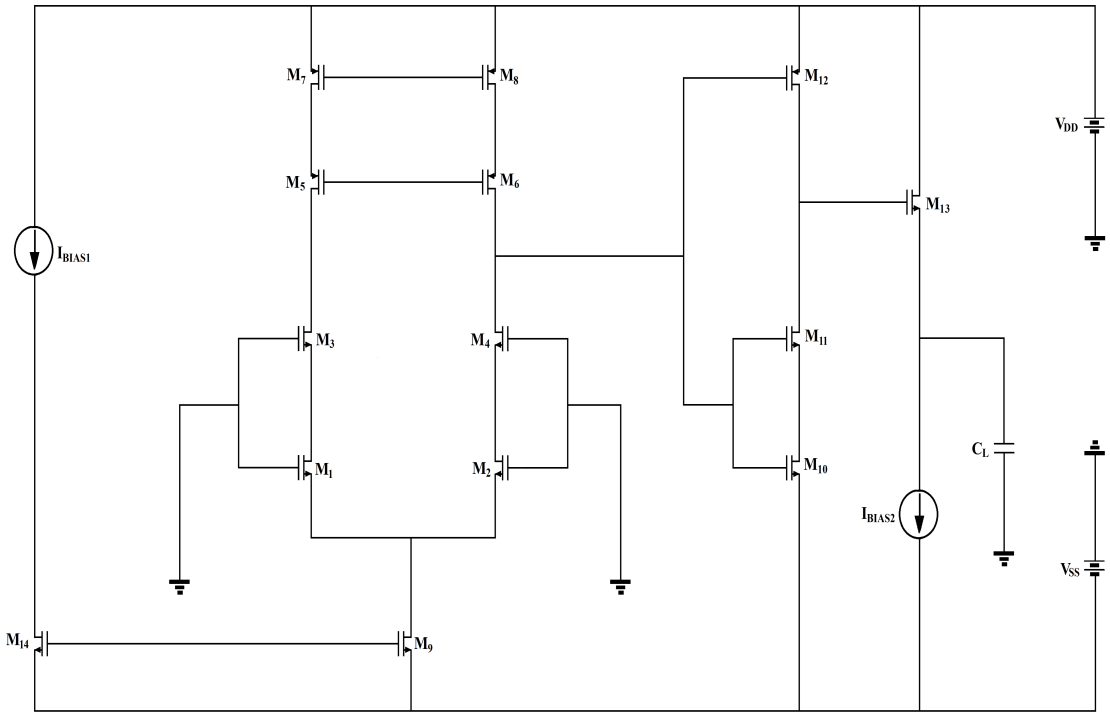

Figure 3.2: Schematic Diagram of a Three-Stage CMOS Op-Amp.

3.1.4 Design Specifications for Three-Stage CMOS Op-Amp Topology

The specifications that are listed in Table 3.2 were used to design a three-stage CMOS operational amplifier.

Table 3.2: Table of Specifications for Three-Stage CMOS.

S.No.	Parameters	Proposed value
1	Technology	$0.18\mu m$
2	Powersupply	$\pm 5V$
3	ICMR	-2.5V to 2.5V
4	Open Loop Gain	$\geq 45dB$
5	Phase Marigin	$\geq 75^0$
6	Unity Gain Bandwidth	$\geq 50MHz$
7	Slew Rate	$\pm 5\frac{V}{\mu s}$
8	DC Power Consumption	$\leq$50mW
9	CMRR	$\geq 40dB$
10	Load Capacitance	15pF

- **GBW**:
  The frequency where the open-loop gain is unity (0dB) is called GBW (also called UGB).[38-41] It is approximately equal to the product of the open-loop gain and dominant pole, which can be expressed as:

$$GBW = A_{OL} \times f_1$$

- g_m**:**
  g_m is a function of device dimensions $\left(\frac{W}{L}\right)$, drain current (I_D) and effective overdrive voltage (V_{eff}), that is

$$g_m = f\left(\frac{W}{L}, I_D, V_{eff}\right) \tag{3.1.14}$$

  where the effective overdrive voltage is given by:

$$V_{eff} = V_{GS} - V_{THN,P} = \sqrt{\frac{2I_{Dn,p}}{\mu_{n,p}C_{OX}\left(\frac{W}{L}\right)_{n,p}}} \tag{3.1.15}$$

where, V_{GS} is gate-to-source voltage, and $V_{THN,P}$ is the threshold voltage, $I_{Dn,p}$ is drain current, $\mu_{n,p}$ is charge carrier mobility in the MOS channel, C_{OX} is gate-oxide capacitance per unit area, $(W/L)_{n,p}$ is the aspect ratio of MOS transistor (W = width and L = length).

g_m of the second (buffer) stage could be obtained as follows:

$$g_{mn,p} = \sqrt{2\mu_n C_{OX} I_{Dn,p} \left(W/L\right)_{n,p}} \tag{3.1.16}$$

Also, from the GBW we have

$$g_m = GBW \times 2\pi C_L \tag{3.1.17}$$

- I_D**:**
  The current expression helps us in calculating $(W/L)_{n,p}$ of the transistors when their I_Ds are known and the overdrive voltage is assigned.

$$I_{Dn,p} = \left(\frac{1}{2}\right) \mu_{n,p} C_{OX} \left(\frac{W}{L}\right)_{n,p} \left(V_{GS} - V_{THN,P}\right)^2 \tag{3.1.18}$$

- **SR:**
  The expression for SR is given by:[43]

$$SR = \left(\frac{dV_{out}}{dt}\right)_{max} \tag{3.1.19}$$

Since the charge on the capacitor Q_{CL} is:

$$Q_{CL} = V_{out} \times C_L$$

$$SR = \frac{1}{C_L} \left(\frac{dQ_{CL}}{dt}\right)_{max}$$

But, the current is defined by

$$I_{CL} = \frac{dQ_{CL}}{dt}$$

Thus, we obtain

$$SR = \frac{I_{CL}}{C_L}$$

The bias current (I_{BIAS2}) is proportional to the current in the output stage which consists of the load capacitor (C_L).

$$SR = \frac{I_{BIAS2}}{C_L} \tag{3.1.20}$$

The tail current, which is equal to I_{D9} goes into transistor M_1 and M_2. Depending on whether the input voltage is positive or negative, each of these two input currents is the average of the tail current (I_{D9}). In other words, under ideal op-amp condition, the bias current (I_{D9}) splits equally through transistors M_1 and M_2, that is $I_{D1} = I_{D2}$, given by:[44]

$$I_{D1} = I_{D2} = \frac{I_{D9}}{2} \tag{3.1.21}$$

Now, determine the sizes of the differential input pair of the circuit (M_1, M_2, M_3 and M_4), by assuming them to be working in saturation mode. Their $(W/L)_n$ could be calculated using I_{D9}.

$$\left(\frac{W}{L}\right)_9 = \frac{I_{D9}}{\mu_n C_{OX}\left(V_{GS} - V_{THN}\right)^2} \tag{3.1.22}$$

$$\left(\frac{W}{L}\right)_{(1,2,3,4)} = \frac{2I_{D(1,2,3,4)}}{\mu_n C_{OX}\left(V_{GS} - V_{THN}\right)^2} \tag{3.1.23}$$

Similarly,

$$\left(\frac{W}{L}\right)_{(5,6,7,8)} = \frac{2I_{D(5,6,7,8)}}{\mu_p C_{OX}\left(V_{GS} - V_{THP}\right)^2} \tag{3.1.24}$$

- **Input/Output Voltage Swing:**
  The output voltage swing represents the range of the output voltage when all the transistors are operated in the active region which can be expressed as:[40]

$$V_{out}^{(+)} = V_{out12} = |V_{DS12}| = \sqrt{\frac{2I_{D12}}{K_N\left(\frac{W}{L}\right)_{12}}} \tag{3.1.25}$$

$$V_{out}^{(-)} = V_{out13} = |V_{DS13}| = \sqrt{\frac{2I_{D13}}{K_P\left(\frac{W}{L}\right)_{13}}} \tag{3.1.26}$$

$$V_{Output\ swing} = V_{DD} + |V_{SS}| - |V_{out13}| - |V_{out12}| \tag{3.1.27}$$

- **PD:**
  For a given supply voltage, we can find the total PD by using:

$$PD = (V_{DD} + |V_{SS}|) \times I_{Total} \tag{3.1.28}$$

$$PD = (V_{DD} + |V_{SS}|) \times (I_{BIAS1} + I_{BIAS2} + I_{D9} + I_{D10}) \tag{3.1.29}$$

3.2 Calculation of Transistor Parameters and sizes

3.2.1 Calculation for Two-Stage CMOS Op-Amp

The aspect ratio of each transistor and other parameters, such as the drain currents of the transistors, transconductance and compensation capacitance are calculated as follows.

1. Estimate the compensation capacitance (C_c): Theoretically, the value of the compensating capacitance is assumed to be from 10 to 22% $\times\ C_L$ to get phase margin $\geq 60°$. For C_L = 10pF, then,

$$C_C = 0.22 \times CL = 0.11 \times 10pF = 1.1pF$$

2. By using the relationship between slew rate (SR), compensation capacitor (C_C) and bias current (I_{D5}), we can obtain:

$$I_{D5} = 2.5\frac{V}{\mu s} \times (1.1pF) = 2.75\mu A$$

   Also, we can obtain the values of $I_{D1} = I_{D2} = I_{D3} = I_{D4} = \frac{I_{D5}}{2} = 1.375\mu$A

3. Determine the transconductance gm1 from C_C and GBW:

$$g_{m1} = 2.305MHz \times 1.1pF \times 2 \times 3.14 = 15.923\mu s$$

4. Calculate the aspect ratios M_1 and M_2, from the values of the transconductance (g_{mn}) and the drain current (I_D):

$$\left(\frac{W}{L}\right)_{1,2} = \frac{g^2 m_1}{2I_{D1}K_n} = \frac{(15.923\mu s)^2}{2 \times 1.375\mu A \times 87.807\frac{\mu A}{V^2}} = 1.049997 \approx 1.05$$

5. Calculate the aspect ratio of transistors M_3 and M_4 from $ICMR_{max}$:

$(V_{GS} - V_{THP}) = (V_{DD} - ICMR_{max}) = 3.5\text{V} - 3.1567\text{V} = 0.3433\text{V}$

$$\left(\frac{W}{L}\right)_{3,4} = \frac{I_{D5}}{K_p(V_{GS} - V_{THp})^2} = \frac{2.75\mu A}{24.1\frac{\mu A}{V^2}(0.117855V^2)} = 0.9683$$

6. Calculate the aspect ratio of transistor M_5 from ICMR_{min}:

$V_{D,SAT} = V_{DD} - ICMR_{min} - V_{GS} = 3.5V - 2.721187V - 0.6448V = 0.134013V$

$$\left(\frac{W}{L}\right)_5 = \frac{2I_{D5}}{K_n(V_{D,SAT})^2} = \frac{2 \times 2.75\mu A}{87.807\frac{\mu A}{V^2}(0.01795V)^2} = 3.4877$$

7. To determine the width of transistor M_6, let us first find g_{m6} as follows:
$g_{m6} \geq 5.5721 \times g_{m1} = 5.5721 \times 15.923\mu s = 88.724246\mu s$
Now, we can find the aspect ratio of M_6:

$$g_{m4} = \sqrt{I_{D4}K_P\left(\frac{W}{L}\right)_4} = \sqrt{1.375\mu A \times 24.1\frac{\mu A}{V^2} \times 0.9683} = 5.6645\mu s$$

$$\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_4 \left(\frac{g_{m6}}{g_{m4}}\right)$$

$$\left(\frac{W}{L}\right)_6 = 0.9683\mu m \times \left(\frac{88.724246\mu s}{5.6645\mu s}\right) = 15.1667$$

$$\left(\frac{W}{L}\right)_6 = \frac{g^2 m_6}{I_{D6}K_p}$$

$$I_{D6} = \frac{g^2 m_6}{\left(\frac{W}{L}\right)_6 K_p}$$

$$I_{D6} = \frac{\left(88.724246\frac{\mu A}{V^2}\right)^2}{15.1667 \times 24.1\frac{\mu A}{V^2}} = 21.53\mu A$$

8. To determine the width of transistor M_7, let us first find g_{m7} as follows:
   $g_{m7} \geq 9.53988 \times g_{m1} = 9.53988 \times 15.923\mu s = 151.9035\mu s$

$$\left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_6 \left(\frac{g_{m7}}{g_{m6}}\right)$$

$$\left(\frac{W}{L}\right)_7 = 15.1667\mu m \times \left(\frac{151.9035\mu s}{88.724246\mu s}\right) = 25.9667$$

$$I_{D6} = I_{D6} = 21.53\mu A$$

9. Determine the aspect ratio of transistor M_8 we use the fact that the value $I_{D8} = I_{D5}$, because M_5 and M_8 are used to form current mirror source (bias string of the circuit). Thus,

$$\frac{I_{D8}}{I_{D5}} = \frac{(\frac{W}{L})_8}{(\frac{W}{L})_5}$$

   Then

$$(\frac{W}{L})_8 = \frac{I_{D8}}{I_{D5}} \times (\frac{W}{L})_5 = (\frac{W}{L})_5 = 3.4877 \approx 3.5$$

10. To determine the width of transistor M_9, let us first find g_{m9} as follows:
    $g_{m9} \geq 14.95578 \times g_{m4} = 14.95578 \times 5.6645\mu s = 84.71701\mu s$

$$\left(\frac{W}{L}\right)_9 = \left(\frac{W}{L}\right)_6 \left(\frac{g_{m9}}{g_{m6}}\right)$$

$$\left(\frac{W}{L}\right)_9 = 15.1667\mu m \times \left(\frac{84.71701\mu s}{88.724246\mu s}\right) = 14.4817$$

    Since M_9 serves as a current buffer, we have $I_{D8} = 0$

Table 3.3 gives summary of calculated values of transistor width and aspect ratios $(W/L)_{n,p}$] for the Two-stage CMOS op-amp.

Table 3.3: $(W/L)_{n,p}$ and width when $L = 0.25\mu m$ for 2-stage:

MOS Transistors	Aspect Ratio, $\left(\frac{W}{L}\right)_{n,p}$	Width, $W(\mu m)$
M_1, M_2	1.05	0.315
M_3, M_4	0.9683	0.2905
M_5	3.4877	1.0463
M_6	15.1667	4.55
M_7	25.9667	7.79
M_8	3.5	1.05
M_9	14.4817	4.3445

3.2.2 Calculation of Transistor Parameters and sizes for Three-Stage CMOS Op-Amp

From the given value of SR we can determine the value of the bias current (I_{BIAS2}):

$$I_{BIAS2} = SR \times C_L = 20V/\mu s \times 10pF = 200\mu A = I_{D12}$$

$(W/L)_{12}$ is:

$$\left(\frac{W}{L}\right)_{12} = \frac{2 \times (200\mu A)}{100\mu A/V^2 \times (0.85V - 0.0335V)^2} = 5.99992 \approx 6.0$$

Since $L_{12} = 0.18\mu m$, we obtain

$$W_{12} = 3.0 \times L_{12} = 3.0 \times 0.18\mu m = 0.54\mu m$$

To find $(W/L)_{14}$, we use $I_{BIAS1} = I_{D14}$:

$$\left(\frac{W}{L}\right)_{14} = \frac{2 \times (100nA)}{100\mu A/V^2 \times (0.85V - 0.8387V)^2} = 15.656$$

Since $L_{14} = 0.18\mu m$, we obtain

$$W_{14} = 15.656 \times L_{14} = 15.656 \times 0.18\mu m = 2.818\mu m$$

The gates of M_9 and M_{14} are connected to one another. So, the tail current $I_{D9} = I_{BIAS1}$ and

$$\left(\frac{W}{L}\right)_{9} = \frac{100nA}{100\mu A/V^2 \times (0.85V - 0.8420082V)^2} = 15.657$$

Since L_9=0.18μm, we obtain

$$W_9 = 15.657 \times L_9 = 15.657 \times 0.18\mu m = 2.818\mu m$$

I_{D1} and I_{D2} can be obtained from I_{D9}:

$$I_{D1} = I_{D2} = \frac{I_{D9}}{2} = \frac{100nA}{2} = 50nA = I_{D3} = I_{D4}$$

To find $(W/L)_{1,2}$, we use

$$\left(\frac{W}{L}\right)_{(1,2)} = \frac{2 \times 50nA}{100\mu A/V^2 \left(0.85V - 0.8432142V\right)^2} = 21.7169$$

Since $L_{1,2}$=L_1=L_2=0.18μm, we obtain

$$W_1 = W_2 = 21.7169 \times L_{1,2} = 21.7169 \times 0.18\mu m = 3.909\mu m$$

To find $(W/L)_{3,4}$, we use $I_{D3} = I_{D4} = 50nA$

$$\left(\frac{W}{L}\right)_{(3,4)} = \frac{2 \times 50nA}{100\mu A/V^2 \left(0.85V - 0.843632V\right)^2} = 24.66$$

Since $L_{3,4}$=L_3=L_4=0.18μm, we obtain

$$W_3 = W_4 = 24.66 \times L_{3,4} = 24.66 \times 0.18\mu m = 4.4388\mu m$$

To find $(W/L)_{5,6}$, we use $I_{D5} = I_{D3} = 50nA$:

$$\left(\frac{W}{L}\right)_{5,6} = \frac{2 \times (50nA)}{50\mu A/V^2 \times [-0.85V - (-0.8378554V)]^2} = 13.56$$

Since $L_{5,6}$=L_5=L_6=0.18μm, we obtain

$$W_5 = W_6 = 13.56 \times L_{5,6} = 13.56 \times 0.18\mu m = 2.4408\mu m$$

To find $(W/L)_{7,8}$, we use $I_{D7} = I_{D5} = 50nA$:

$$\left(\frac{W}{L}\right)_{7,8} = \frac{2 \times (50nA)}{50\mu A/V^2 \times [-0.85V - (-0.7873776V)]^2} = 0.51$$

Since $L_{7,8}$=L_7=L_8=0.18μm, we obtain

$$W_7 = W_8 = 0.51 \times L_{7,8} = 0.51 \times 0.18\mu m = 0.0918\mu m$$

From the GBW we have

$$g_{m13} = GBW \times 2\pi C_L = 43.557MHz \times 2\pi \times 10pF = 2.7354mS$$

Calculate $(W/L)_{13}$ to achieve the desired GBW:

$$\left(\frac{W}{L}\right)_{13} = \frac{(2.7354mS)^2}{2 \times I_{D13} \times 50\mu A/V^2}$$

Also,

$$\left(\frac{W}{L}\right)_{13} = \frac{2 \times I_{D13}}{50\mu A/V^2 \times [-0.85V - (-2.8321598V)]^2}$$

$$\frac{(2.7354mS)^2}{2 \times I_{D13} \times 50\mu A/V^2} = \frac{2 \times I_{D13}}{50\mu A/V^2 \times [-0.85V - (-2.8321598V)]^2}$$

$$(2 \times I_{D13})^2 = (2.7354mS \times 1.9821598V)^2$$

$$I_{D13} = 2.711mA$$

Thus,

$$\left(\frac{W}{L}\right)_{13} = \frac{(2.7354mS)^2}{2 \times 2.711mA \times 50\mu A/V^2} = 27.6$$

Since L_{13}=0.18μm, we obtain

$$W_{13} = 27.6 \times L_{13} = 27.6 \times 0.18\mu m = 4.968\mu m$$

To find $(W/L)_{11}$, we use $I_{D11} = I_{D13} = 2.711mA$:

$$\left(\frac{W}{L}\right)_{11} = \frac{2 \times 2.711mA}{100\mu A/V^2 \times (0.85V - 2.92441V)^2} = 12.59999 \approx 12.6$$

Since L_{11}=0.18μm, we obtain

$$W_{11} = 12.6 \times L_{11} = 12.6 \times 0.18\mu m = 2.268\mu m$$

To find $(W/L)_{10}$, we use $I_{D10} = I_{D11} = 2.711mA$:

$$\left(\frac{W}{L}\right)_{10} = \frac{2 \times 2.711mA}{100\mu A/V^2 \times (0.85V - 3.788326V)^2} = 6.27999 \approx 6.28$$

Since L_{10}=0.18μm, we obtain

$$W_{10} = 6.28 \times L_{10} = 6.28 \times 0.18\mu m = 1.1304\mu m$$

Table 3.4 gives summary of calculated values of transistor width and aspect ratios $(W/L)_{n,p}$] for the Three-stage CMOS op-amp.

Table 3.4: $(W/L)_{n,p}$ and width when $L = 0.18\mu m$ for 3-stage:

MOS Transistors	Aspect Ratio, $\frac{W}{L}$	Width, $W(\mu m)$
M_1, M_2	21.7169	3.909
M_3, M_4	24.66	4.4388
M_5, M_6	13.56	2.4408
M_7, M_8	0.51	0.0918
M_9, M_{14}	15.656	2.818
M_{10}	6.28	1.1304
M_{11}	12.6	2.268
M_{12}	3.0	0.54
M_{13}	27.6	4.968

Chapter 4

DESIGN AND SIMULATION

In this chapter, first the design, simulation and data analysis for the two-stage CMOS op-amp with current buffer was discussed. Then, the design, simulation and data analysis for the three-stage CMOS op-amp will be discussed.

4.1 Circuit Design for Two-Stage CMOS Op-Amp

The two stage CMOS operational amplifier with current buffer circuit design, simulation and analysis were carried out based on the proposed schematic layout given in figure 3.1. The final design with appropriate device sizes and adding input offset voltage (V_{IO}) is shown in Fig.4.1.

4.2 Bias Point Analysis

During DC analysis, the bias point is used to measure the operating point of the design, like bias point voltage, bias point current, and power dissipation at which it can be adjusted by the input offset voltage to obtain minimum output offset voltage.

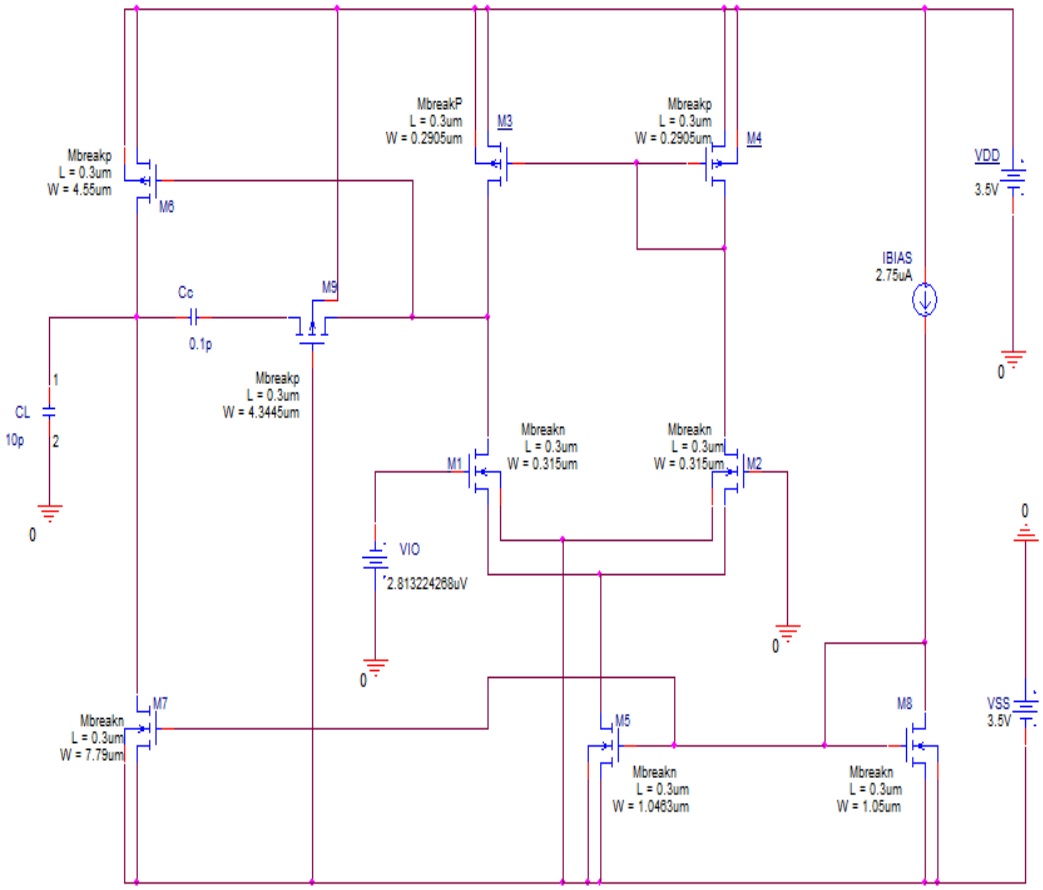

Figure 4.1: Two Stage CMOS Op-Amp with Current Buffer Circuit Design

4.2.1 Node voltages:

The bias point voltages are the voltages across each transistor and capacitor in the circuit shown in Fig.4.2. The output offset voltage is equal to the voltage across the load capacitor ($V_{out,\ offset} = V_{CL}$) which was reduced to a very small value of 129.1nV by connecting an appropriate DC input offset voltage of V_{IO}.

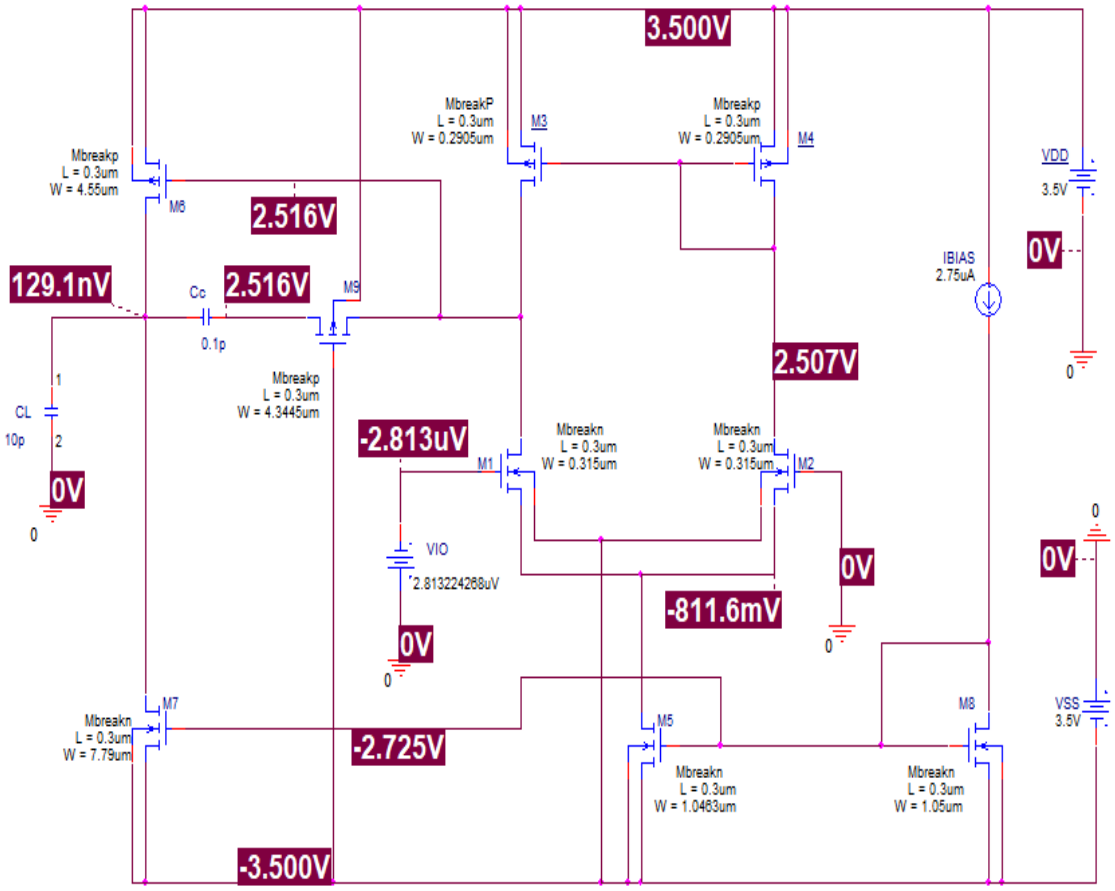

Figure 4.2: Simulation Results of Bias Point Voltages for the two-stage

4.2.2 Bias point currents:

The bias point current analysis is done to determine the drain currents of every transistor. Fig.4.3 shows the simulation results of bias point currents. One can observe from Fig.4.3 that the bias current I_{BIAS} and the tail current (I_{D5}) are equal: $2.75\mu A$, which is also equal to I_{D8}. In addition, we can see that: $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1.3757\mu A = I_{D5}/2$; $I_{D6} = I_{D7} = 20.51\mu A$, and $I_{D9} = 129.8{\times}10^{-21}$A.

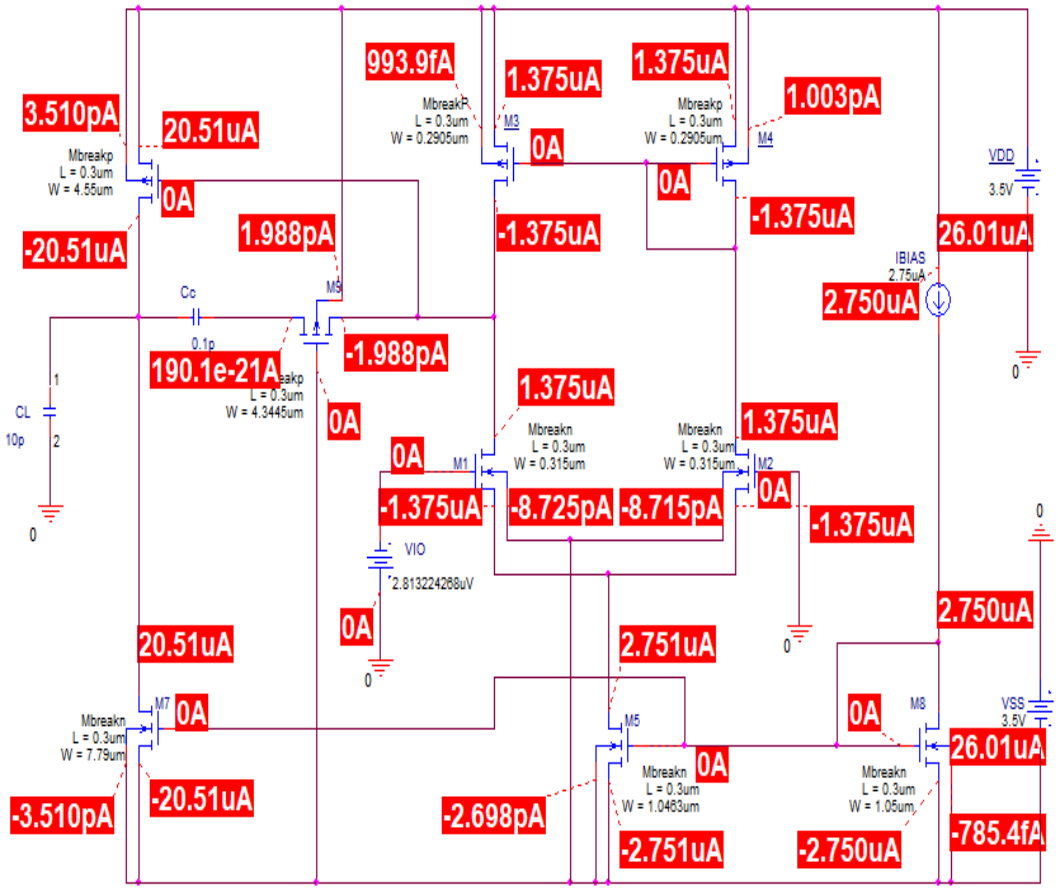

Figure 4.3: Simulation Results of Bias Point Currents for the two-stage

4.2.3 Power dissipation:

Fig.4.4 shows the simulation result for the power dissipation of the two stage CMOS op-amp with current buffer circuit. The total power dissipation (P_D) of the circuit is given by:

$P_D = (71.8 + 71.8 + 0.000001956 + 1.353 + 1.366 + 4.577 + 4.564 + 7.395 + 17{,}12 + 2.133)\mu W \approx 0.1821\text{mW}$

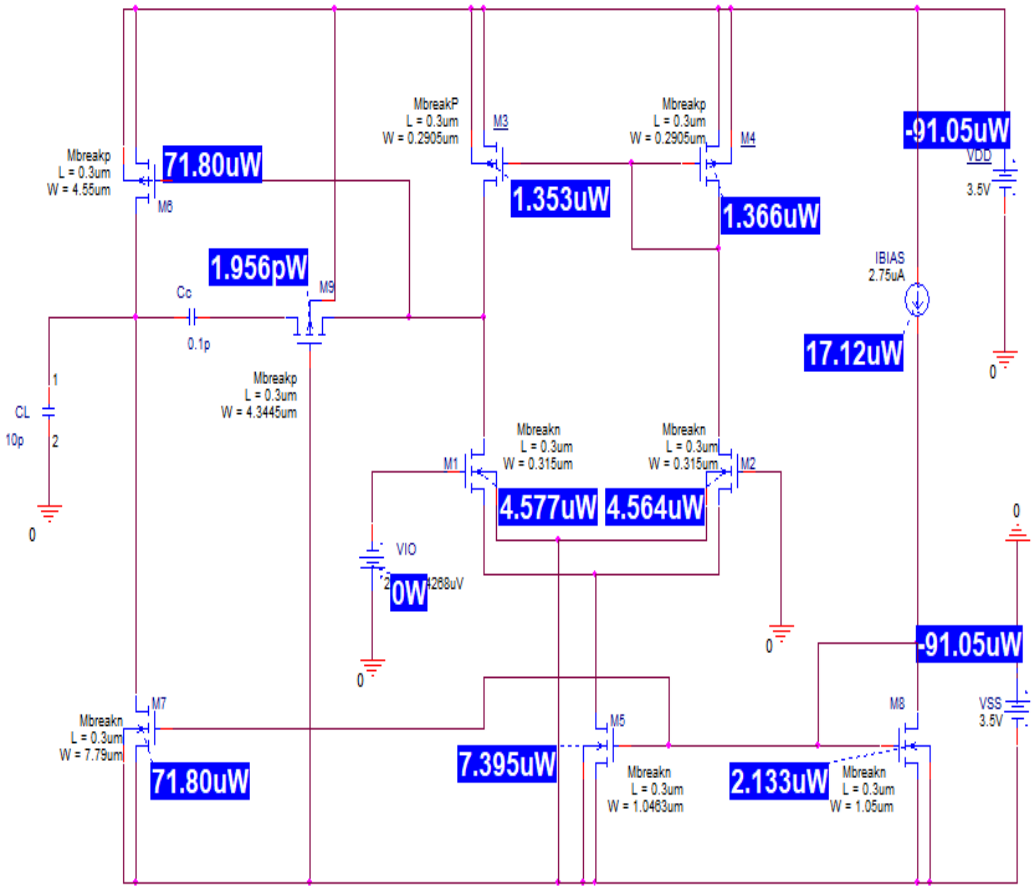

Figure 4.4: Simulation Results of Power Dissipation.

4.3 AC Sweep/Noise Analysis

The AC Sweep/Noise analysis varies the operating frequency in a linear or logarithmic manner. It linearizes the circuit around the DC operating point and then calculates the network variables as functions of frequency. The DC open loop gain, UGB and Phase Margin are obtained by using AC Sweep/Noise analysis.

4.3.1 Open loop gain, UGB and Phase Margin:

The circuit design for the open loop gain is shown in Fig.4.5.

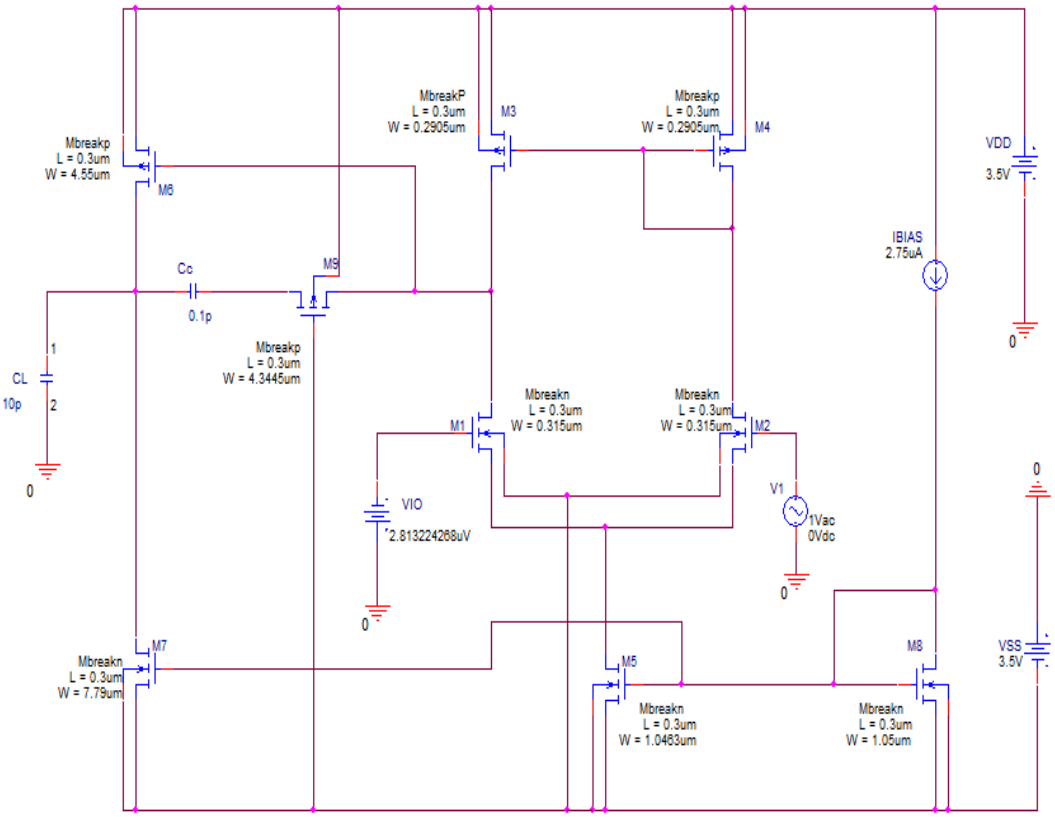

Figure 4.5: Circuit Design for Open Loop Gain, UGB and Phase Margin for the two-stage

AC sources are time dependent and the circuit has input small signals as a function of frequency applied to the input terminal(s). The output value of the AC signal varies over a range of frequency in phase or out of phase with the input values of the AC signal. In this configuration, the amplifier is an open loop with ±3.5V supply voltages. An AC signal of 1V magnitude is applied at the noninverting input terminal.

Fig.4.6 is graph of open loop gain, UGB and phase margin obtained from the simulation. The open loop gain is found to be 133.33dB. The -3dB cut-off frequency and the UGB are 5.88Hz and 6.87MHz, respectively. The phase margin is 73.631^0.

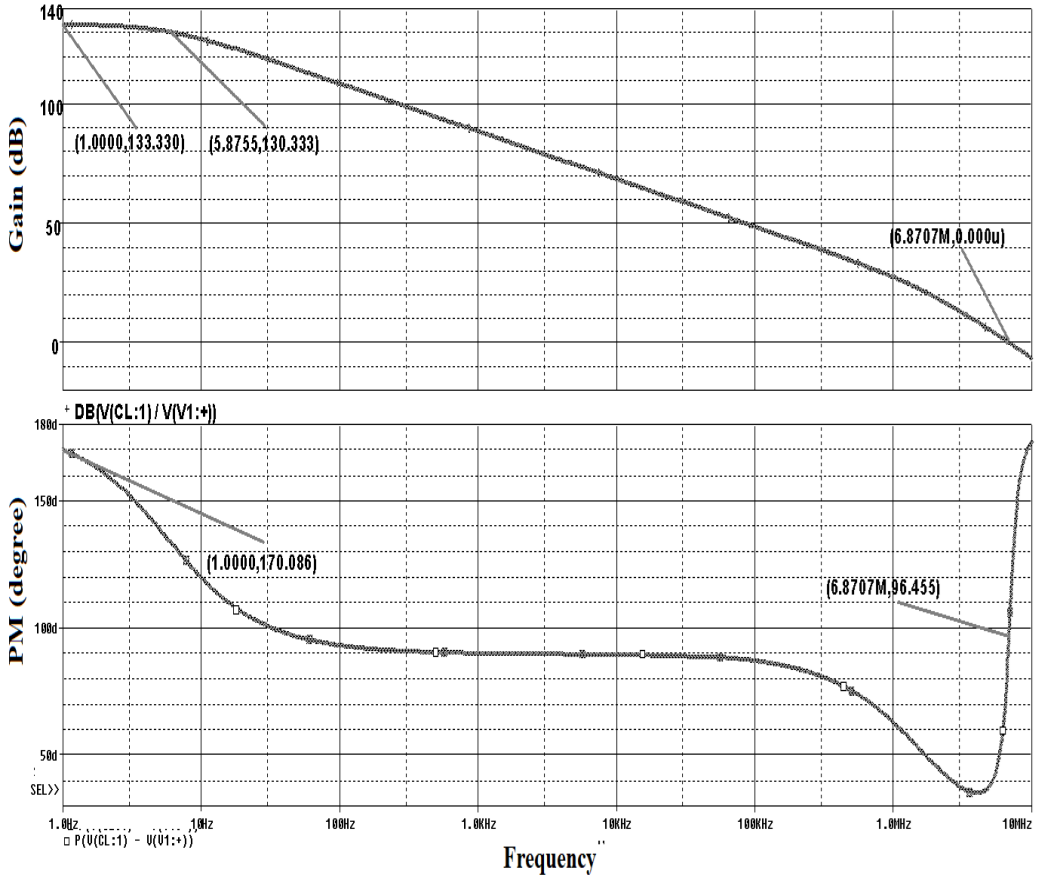

Figure 4.6: Simulation Result for Open Loop Gain, UGB and Phase Margin for the two-stage

4.4 Time Domain (Transient) Analysis

Time domain (transient) analysis is probably the most popular analysis. AC sources are time dependent and the circuit has small signal applied to its input terminal(s). The output value of the AC signal tries to follow the input signal without distortion

or clipping for some amplitudes of the input AC signal. The input/output voltage swing is obtained by using Time Domain (Transient) analysis.

4.4.1 Input/output Voltage Swing:

The circuit design for the analysis of the input/output voltage swing is shown in Fig.4.7. A sinusoidal input signal of $22.5\mu V$, 200Hz frequency is connected to the inverting terminal.

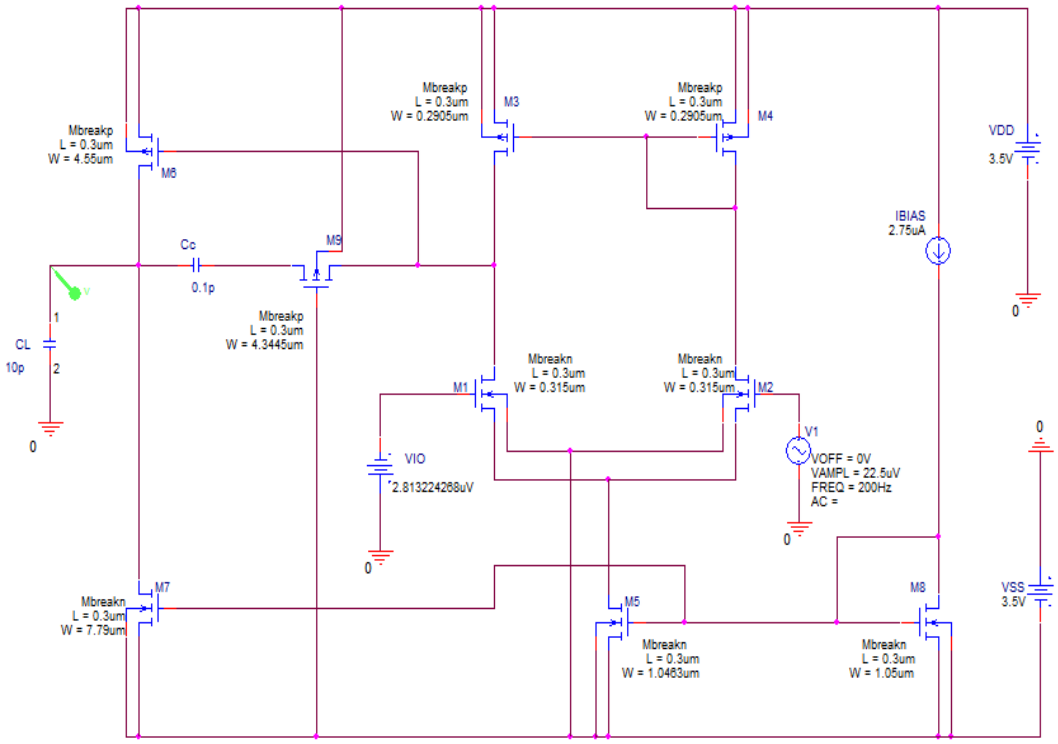

Figure 4.7: Circuit Design to Measure the Input/Output Voltage Swing for the two-stage

From Fig.4.8 simulation results of the input/output voltage swing, we can observe that when the peak-to-peak input AC voltage swing is $45\mu V$, the peak-to-peak output AC voltage swing is 6.0417V.

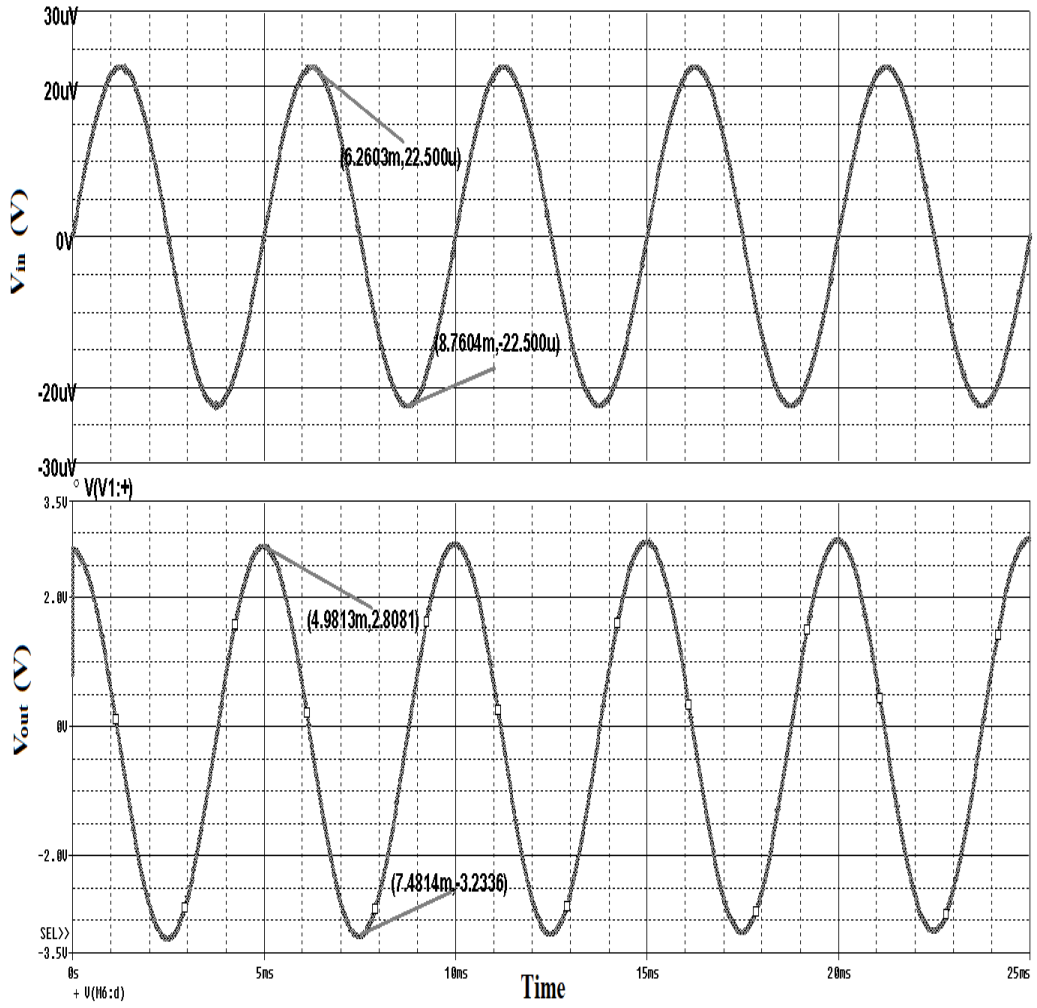

Figure 4.8: Simulation Result of Input/output Voltage Swing for the two-stage

The gain from the input/output voltage swings can be calculated as follows:

$$Gain = \frac{V(out, peak - to - peak)}{V(in, peak - to - peak)}$$

$$Gain = \frac{6.0417V}{45\mu V} = 134,260$$

In decibel scale (dB), this gain is:

$$Gain = 20log(134,260) = 102.56dB$$

4.5 Circuit Design for Three-Stage CMOS Op-Amp

We have designed a three - stage CMOS op-amp using the layout proposed in Fig.3.2 and $(W/L)_{n,p}$ tabulated in Table 3.3. Fig.4.9 shows the design for the three - stage CMOS op-amp circuit.

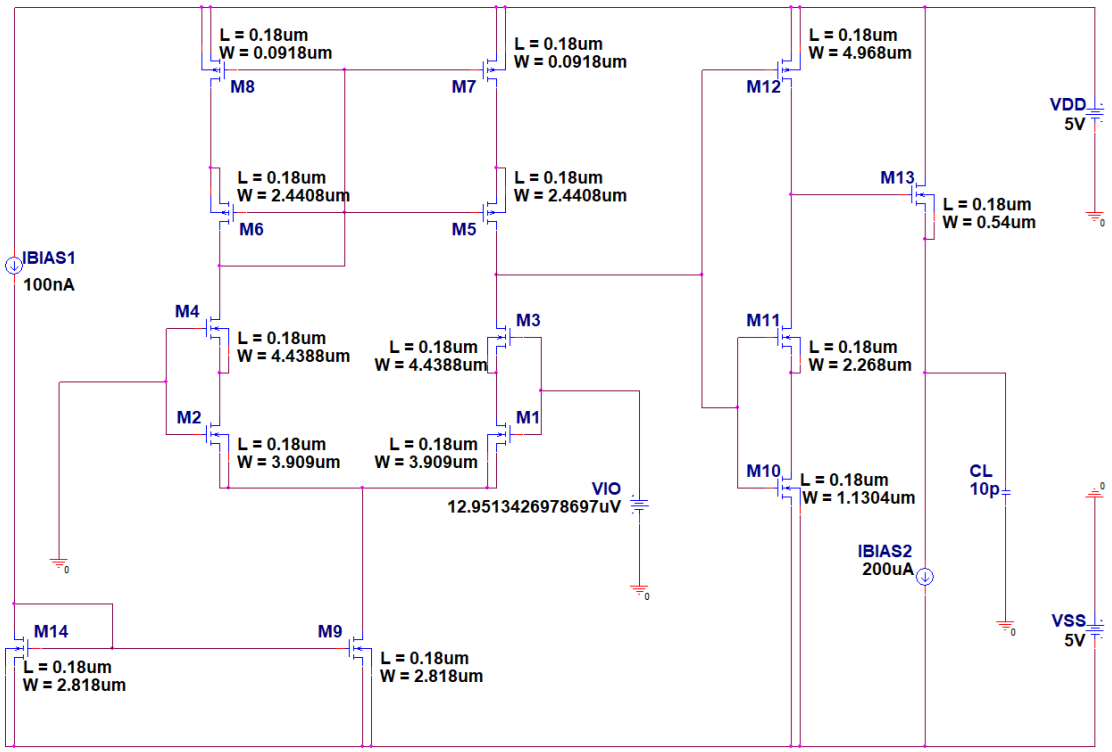

Figure 4.9: Three - Stage CMOS Op-Amp Circuit Design

4.6 Simulation and Data Analysis

4.6.1 DC Analysis

A. Node Voltages

The node voltage simulations are shown in Fig.4.10. From the figure, we observe that the output offset voltage is 79.54nV, which is very small.

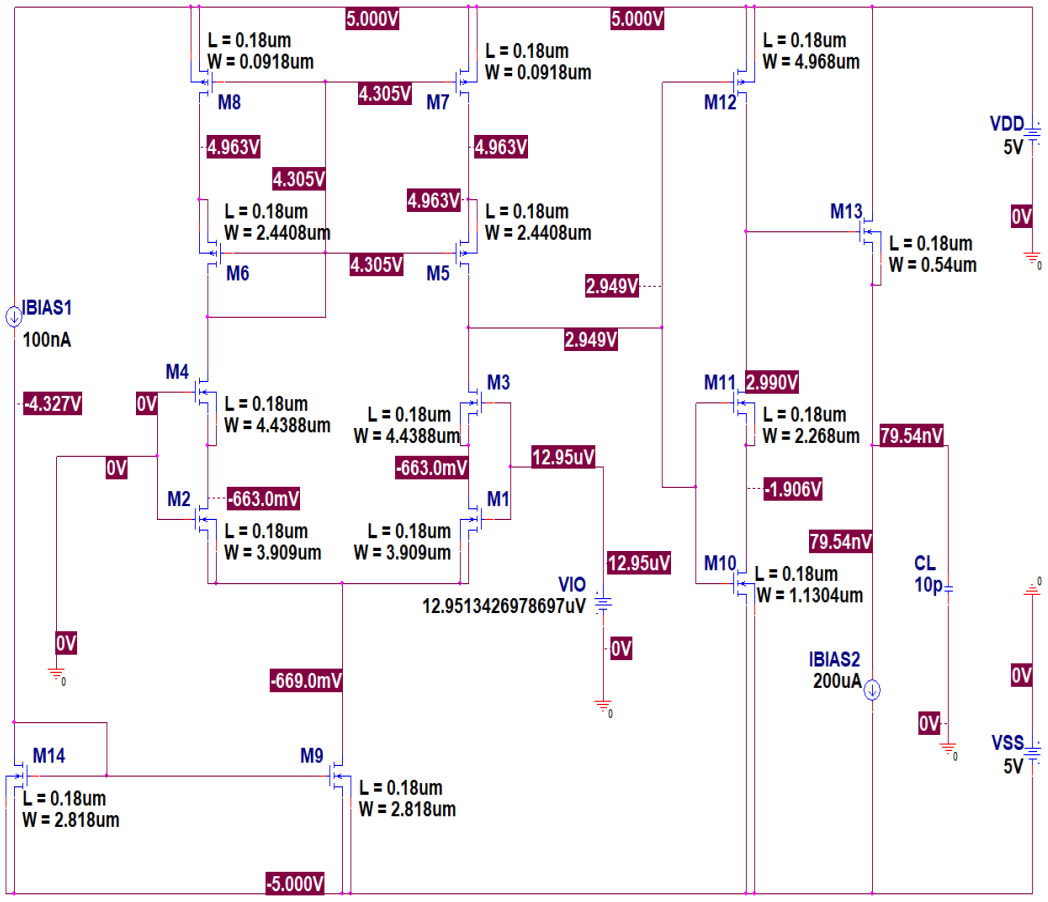

Figure 4.10: Simulation Results of Output Offset Voltage for the three-stage

B. Node Currents

Fig.4.11 shows the simulation results of node currents. $I_{D9} = 100.7nA$. For the first stage MOS transistors, $I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_{D5} = I_{D6} = I_{D7} = I_{D8} = I_{D9}/2 = 50.37nA$. $I_{D14} = 100nA = I_{BISA1}$. For the second (buffer) stage MOS transistors, $I_{D10} = I_{D11} = I_{D12} = 2.711mA$. For the third (output) stage MOS transistor, $I_{D13} = 200\mu A = I_{BISA2}$. Thus, one can observe that I_Ds of all MOS transistors are equal to those predicted in chapter 3 using hand calculations.

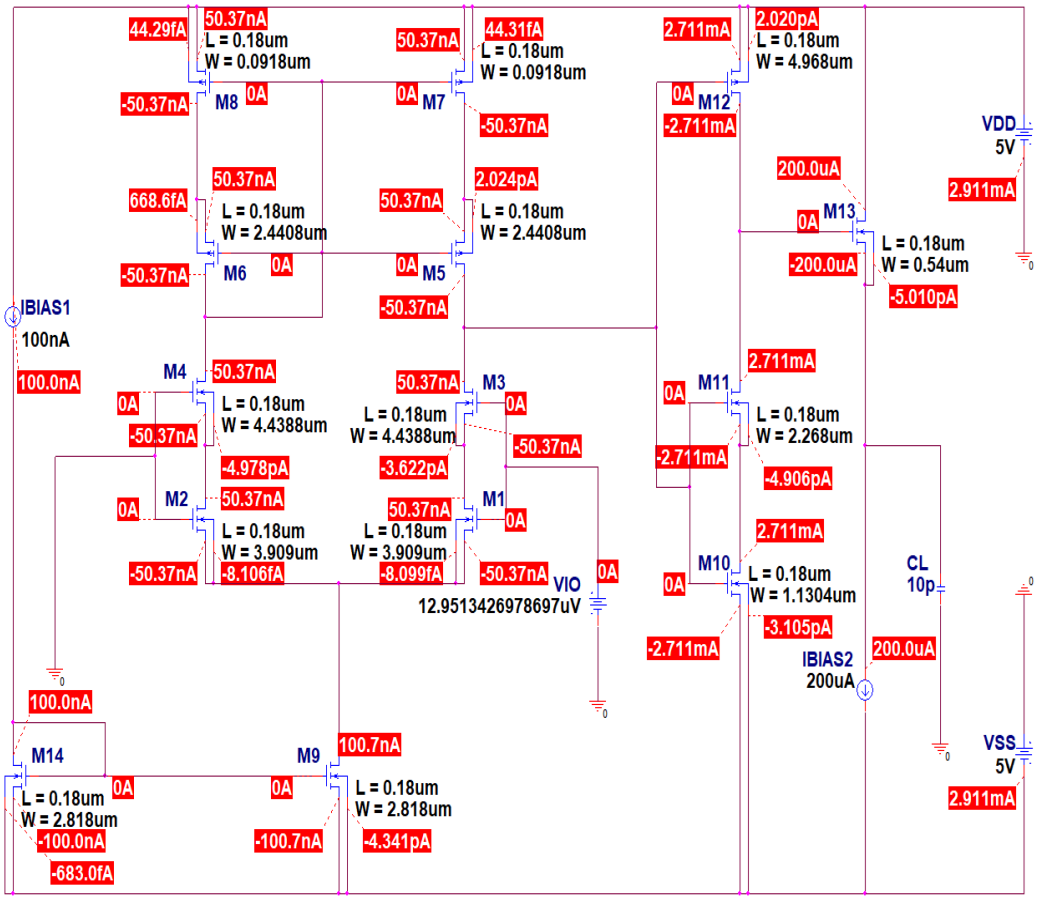

Figure 4.11: Simulation Results of Node Currents for the three-stage

C. PD

Fig.4.12 shows the simulation results of the PD across each MOSFET.

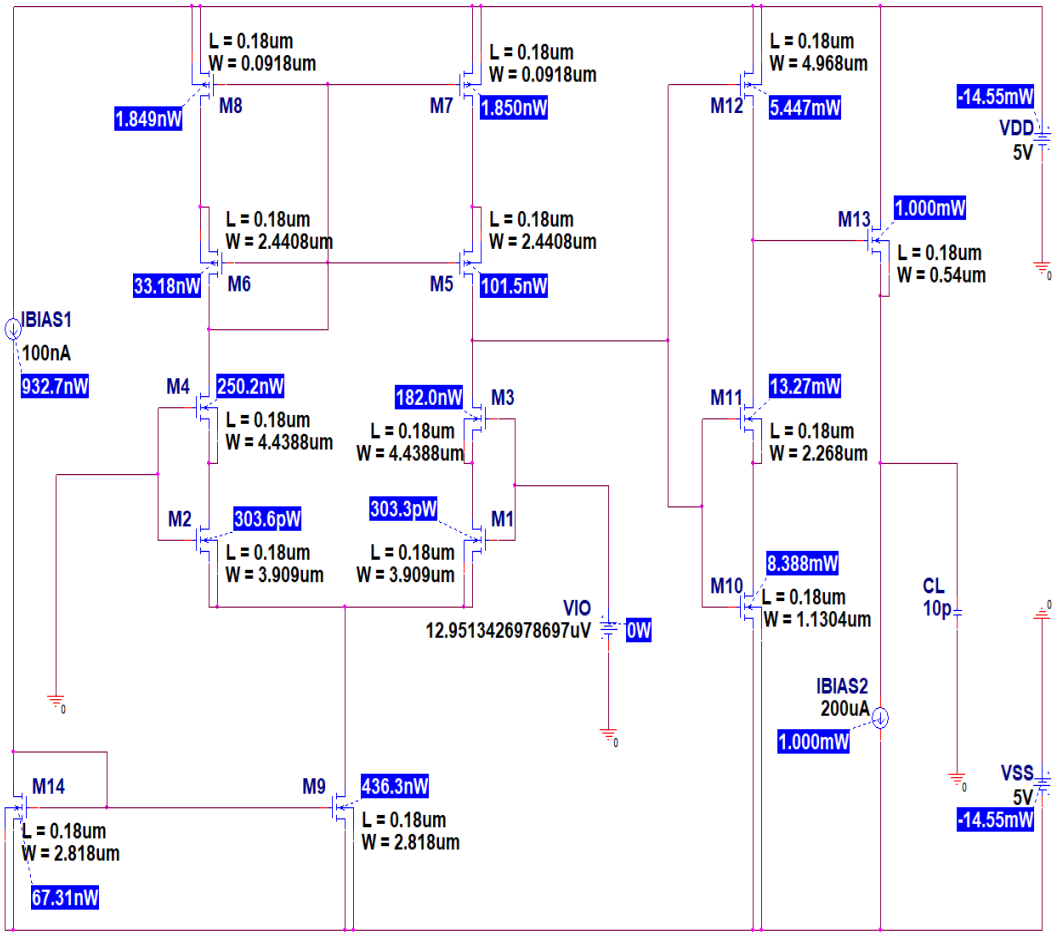

Figure 4.12: Simulation Result of PD for the three-stage

The total PD of the circuit is:

$$PD = (932.7 + 67.31 + 1.849 + 1.85 + 33.18 + 101.5+)\, nW+$$
$$(250.2 + 182 + 0.0003036 + 0.0003033 + 436.3+)\, nW+$$
$$(5.447 + 13.27 + 8.388 + 1 + 1)\, mW = 29.107mW$$

4.6.2 AC Analysis

GBW and Open Loop Gain

The open loop gain, GBW and PM are measured using the circuit design shown in Fig.4.13.

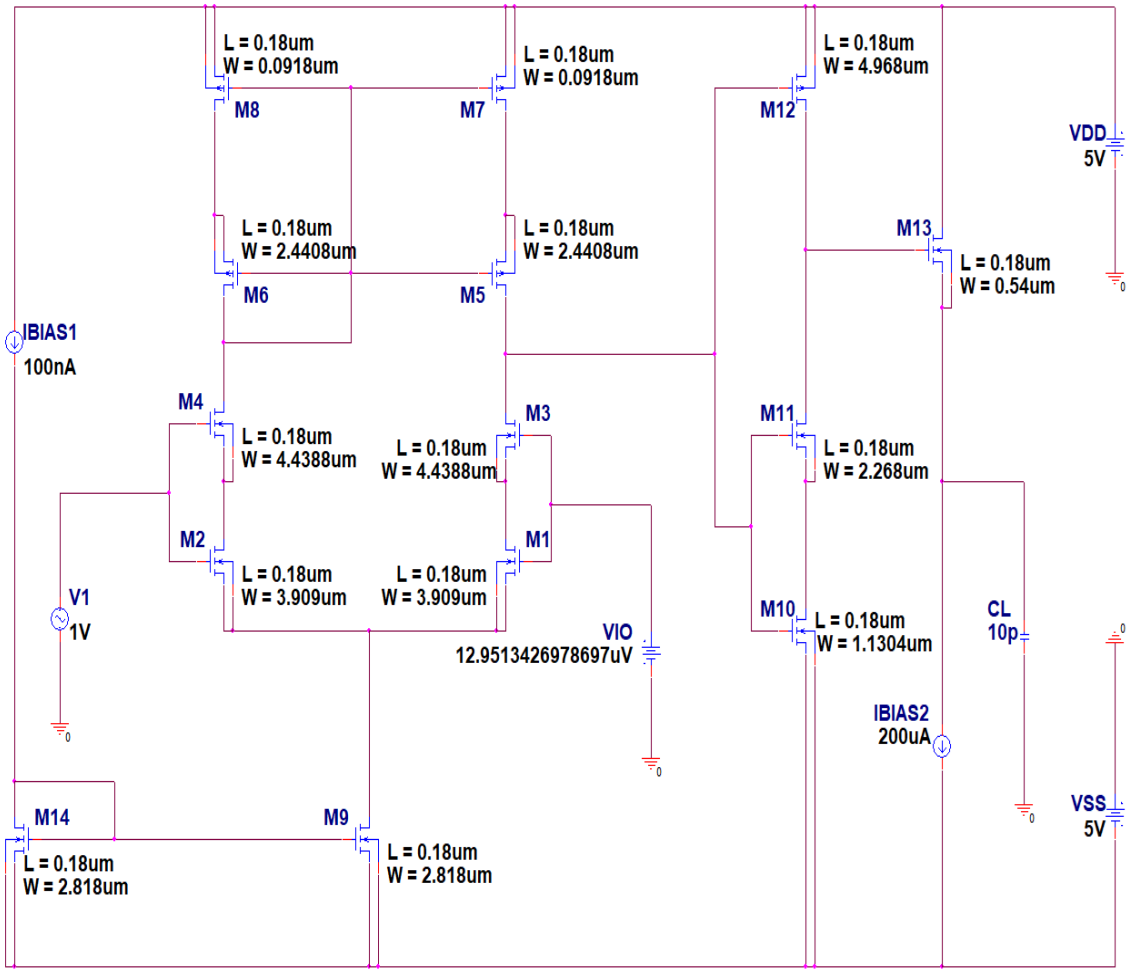

Figure 4.13: Circuit Design to Measure Gain, GBW and PM for the three-stage

The simulation result of the Gain, GBW and PM is shown in Fig.4.14. As we can see from the graph, the gain is 156.548dB, GBW is 428.667MHz and PM is 67.07^0.

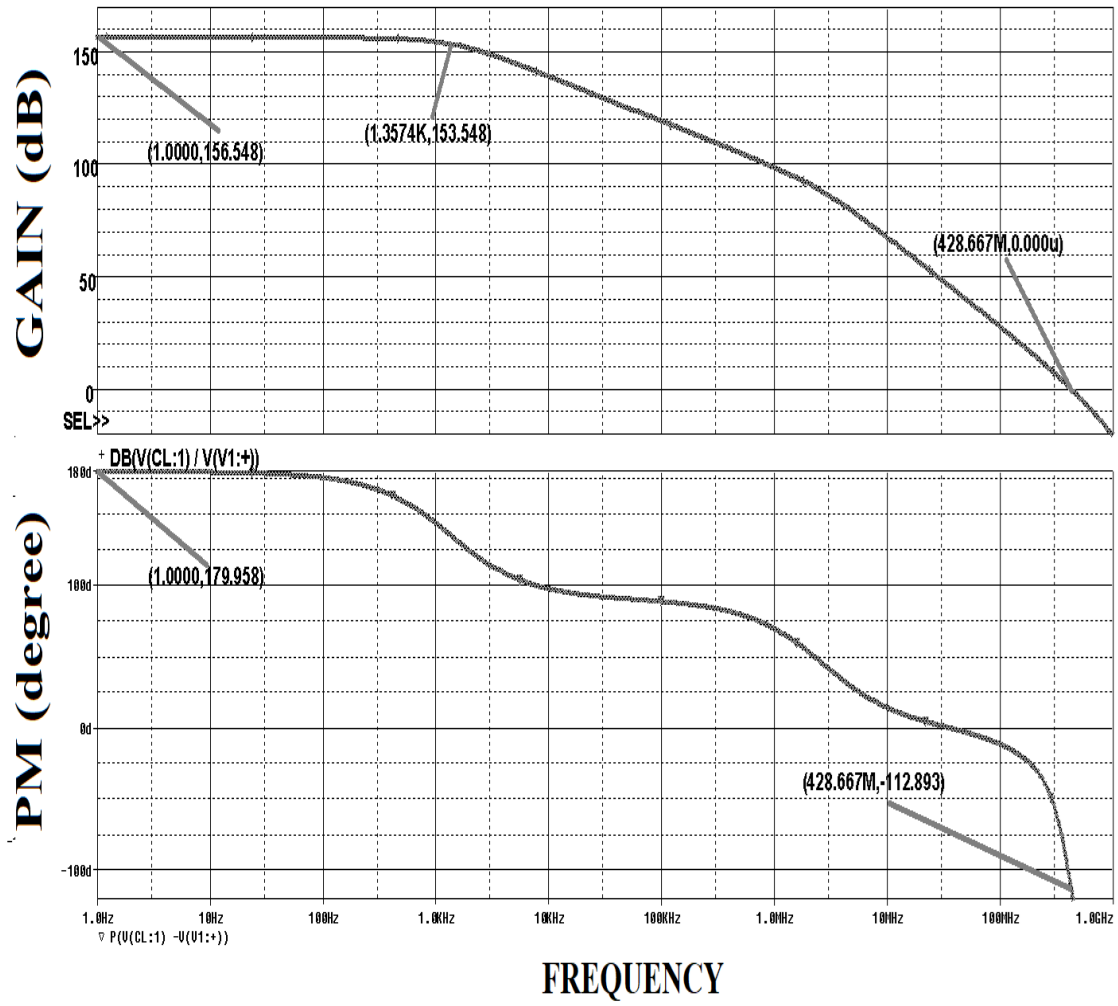

Figure 4.14: Simulation Result of Gain, GBW and PM for the three-stage

Input and Output Voltage Swings

The circuit design to measure the input/output voltage swing is shown in Fig.4.15. A sinusoidal voltage of 439nV amplitude and 200Hz frequency is connected to the inverting terminal of the op-amp.

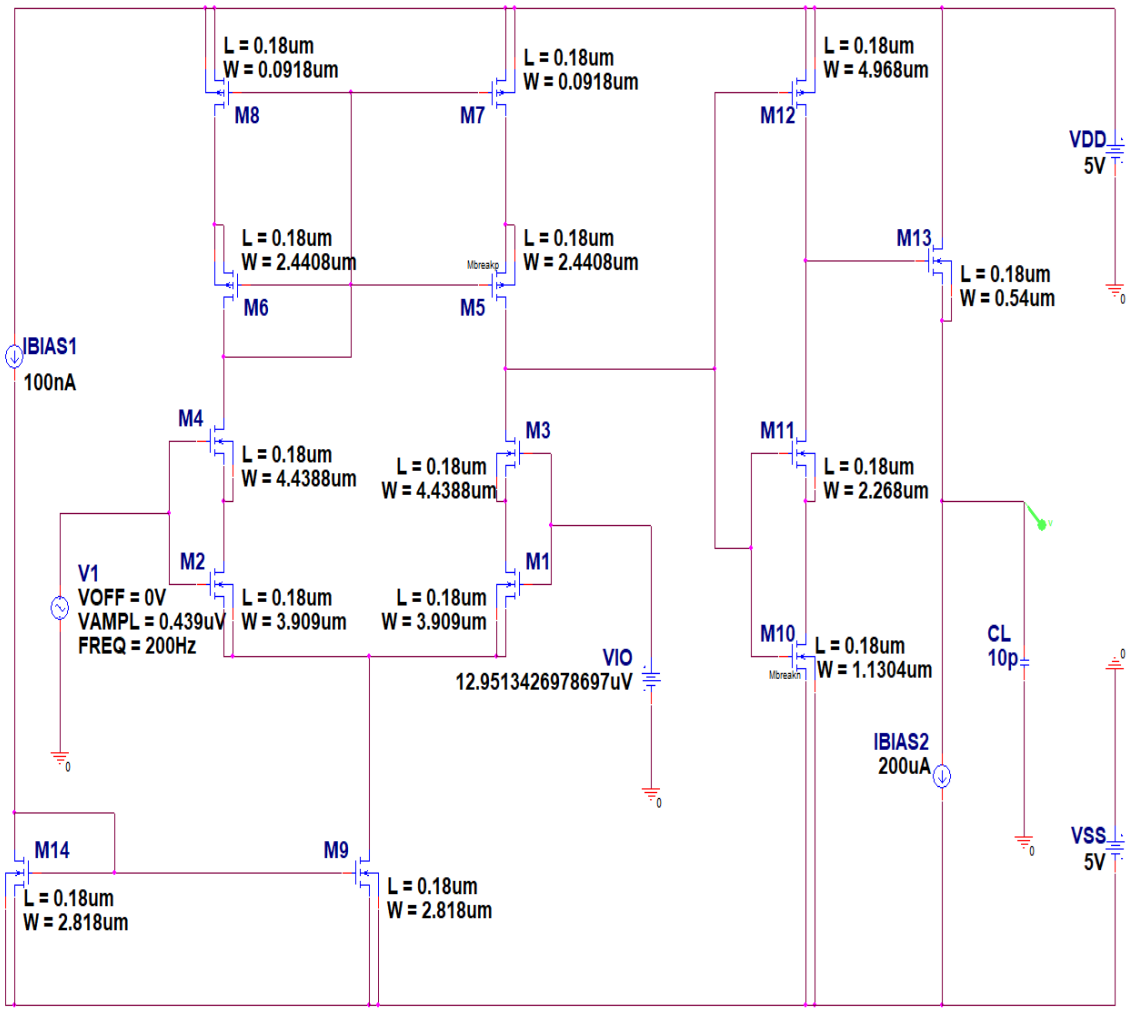

Figure 4.15: Circuit Design to Measure the Input/Output Voltage Swings for the three-stage

Fig.4.16 shows the simulation results of the input and output voltage swings. When the peak-to-peak input signal is 878nV, the peak-to-peak output signal was found to be 1,227.576mV.

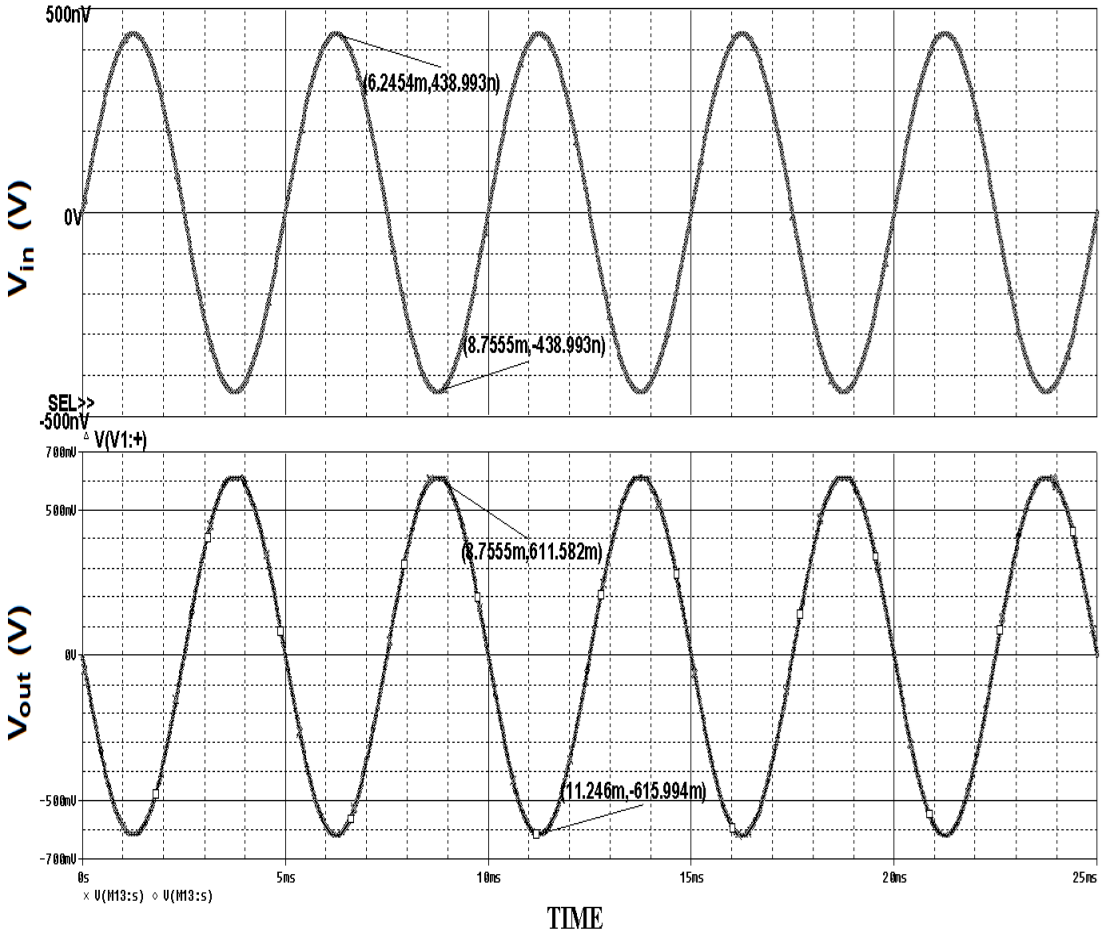

Figure 4.16: Simulation Result of Input and Output Voltage Swings for the three-stage

The gain from the input/output voltage swings can be calculated as follows:

$$Gain = \frac{V(out, peak - to - peak)}{V(in, peak - to - peak)}$$

$$Gain = \frac{1,227.576mV}{878nV} = 1,398,150.34$$

In decibel scale (dB), this gain is:

$$Gain = 20log(1,398,150.34) = 122.91dB$$

Table 4.1: **Summary of proposed values and simulation results for 2-stage**

Parameter	Proposed value	Simulation Result
Open loop gain	$\geqslant 80dB$	133.33dB
UGB	$\geq 2.305MHz$	6.87MHz
PM	$\geqslant 60^0$	73.63^0
Gain from Voltage swing	NA	102.56dB

Table 4.2: **Summary of proposed values and simulation results for 3-stage**

Parameter	Proposed value	Simulation Result
Open loop gain	$\geqslant 80dB$	156.55dB
UGB	$\geq 43.557MHz$	428.67MHz
PM	$\geqslant 60^0$	67.1^0
Gain from Voltage swing	NA	122.91dB

Chapter 5

CONCLUSION AND RECOMMENDATIONS

5.1 Conclusion

This research presented a systematic performance evaluation of a three-stage CMOS op-amp versus a two-stage CMOS op-amp with current buffer against the DC open loop gain and voltage swing, simulated via Cadence OrCAD and Allegro SPB v17.4. The results obtained demonstrates that the three-stage CMOS op-amp has architecture achieves extremely wide GBW, which is two order of magnitude higher than that of the two-stage op-amp. This result will make using the design for much higher frequency ranges. Also, the three-stage CMOS op-amp has an exceptionally high DC open loop gain than that of the two stage CMOS op-amp and the gain obtained from the input/output voltage swing was also high for the three-stage CMOS op-amp, which could be very useful for amplifying week signals.

5.2 Recommendation

We recommend that, other performance parameters, such as ICMR, SR, CMRR, and PSRR should also be studied for complete analysis of the two design topologies.

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Declaration

I, hereby declare that this thesis is my original work and has not been presented for a degree in any other university, and that all sources of materials have been duly acknowledged.

Name: Tadesse Baye

Signature: ———————

Date: ———————

This thesis has been submitted for the examination with my approval as a University advisor.

Name: Dr Haileeyesus Workineh

Signature : ———————

Date: ———————