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SINGLE ENDED OUTPUT FOLDED CASCODE CMOS OPERATIONAL AMPLIFIER



A THESIS SUBMITTED TO
THE DEPARTMENT OF PHYSICS OF
BAHIR DAR UNIVERSITY

IN PARTIAL FULFILLMENT OF THE
REQUIREMENTS FOR THE DEGREE OF
MASTER OF SCIENCE IN PHYSICS

By

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BAHIR DAR, ETHIOPIA

JANUARY 2021

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COLLEGE OF SCIENCE
DEPARTMENT OF
PHYSICS

The undersigned hereby certify that they have read and recommend to the Faculty of Graduate Studies for acceptance a graduate thesis work entitled “**SINGLE ENDED OUTPUT FOLDED CASCODE CMOS OPERATIONAL AMPLIFIER**” by **YOHANNES ADDIS** in partial fulfillment of the requirements for the degree of **Master of Science in Physics**.

Dated: January 2021

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CMOS OPERATIONAL AMPLIFIER**

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This page is dedicated to My family ...

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Abstract

The main task of this research is to design and simulate single-ended output folded cascode CMOS op amp by using OrCAD PSPICE Design and Simulation software based on analog and digital electronic devices and advanced integrated circuit design fundamentals. It involves three basic concepts, theoretical calculation, design, and simulation verification using OrCAD PSPICE software. The single-ended output folded cascode CMOS op amp was analyzed by considering the effects of aspect ratios on the characteristics of the design parameters such as, nodal analysis, DC sweep (node voltage, node current, PD), transient analysis (Input/Output Voltage Swing and Slew Rate) and AC Sweep (DC open loop gain, UGB, CMRR). The simulation results show that the design of the single-ended output folded cascode CMOS op amp has an open loop gain of 54.013dB, CMRR of 52.138dB, unity gain frequency of 14.032MHz, slew rate of $2.081V/\mu s$, and ICMR of 516.000mV to 517.000V. A 5pF load capacitor is applied in performing a stable phase margin of 67.336° . It operates at 2.5V power supply with a very low power dissipation of 0.035379mW

Key Words: Folded cascode, PD, ICMR, Open loop gain, CMRR and OrCAD PSPICE.

Abbreviations Used

Abbreviation	Expanded form
A_{CM}	common mode gain
gm	transconductance
Op Amp	operational Amplifier
I_D	drain current
PM	phase margin
t_{ox}	Oxide thickness
V_{DD}	drain-Drain current
W/L	Aspect ratio
μ_n	Electron mobility
μ_p	hole mobility
MOSFET	metal oxide semiconductor field effect transistor
CMOS	complementary metal oxide semiconductor
I_S	source current
NMOS	negative channel MOSFET
PMOS	positive channel MOSFET
A_{DM}	differential mode gain
V_{DS}	drain source voltage
dB	decibel
GBW	gain band width
IC	integrated circuit
SPICE	Simulation Program for Integrated Circuit Enhancement
SR	slaw rate
ϵ_{OX}	Permittivity of oxide
AC/DC	analog to digital conversion

Chapter 1

INTRODUCTION

1.1 Background of the Study

The history of op amp began in the days of vacuum tubes. The circuit was constructed such that the characteristics of the overall amplifiers were largely determined by the type and amount of feedbacks. Thus, the differential amplifier itself had become a building block that could function in different operations by altering the feedback. Some of the operations that were used included adding, multiplying, and logarithmic operations. The evolution of op amp continued through the transistor era and continued to decrease in size and increase in performance. The earliest versions of op amp were designed from many resistors, capacitors and MOSFET transistors. Especially resistors take much more area than the others. MOSFET transistors take less area and power dissipation as a result they will give us a high gain op amp. So, researchers have replaced the resistors by MOSFET transistors and two capacitors. Recent progresses in Very Large Scale Integration (VLSI) technologies have made possible the realization of complete systems on a single chip. Since complete systems often include analog devices as well as digital devices, there has been a reemergence of interest in Metal-Oxide Semiconductor (MOS) analog circuits.

Complementary Metal-Oxide-Semiconductor (CMOS) technology is a circuit implementation using both PMOS and NMOS transistors on the same silicon chip. Op amp with gain controlled by negative feedback were first thought of in the 1930 as a way of creating amplifiers for the telephone system. The evolution continued through molded or modular devices and finally in the mid 1960s a complete operational amplifier was integrated into a single integrated circuit (IC) package. About 33 years later

CMOS was developed in 1963 by Fran Wan Lass and Chin-Tang Shan of Fair Child to overcome the drawbacks of PMOS and NMOS [1]. Folded cascode architecture is used for high swing and high gain with low power consumption. This op-amp uses cascodeing in the output stage [2]. Op-amps are circuit elements that are used to amplify the magnitude of any input signal at the output. The op-amp is a versatile device that can be used to amplify DC as well as AC input signals. An op amp produces an output voltage that is typically hundreds of thousands times larger than the voltage difference between its input terminals [3]. Op amps are built with different complexity levels to be used to realize functions ranging from a simple DC bias generation to high speed amplifications, oscillators, waveform generators and also for performing mathematical operations such as addition, subtraction, integration and differentiation[4].

The op amp is mostly used in feedback configuration[5]. The primary requirement of an op amp is to have an open-loop gain that is sufficiently large to implement the negative feedback concepts[6]. CMOS Op-amp can be used efficiently for practical applications; for example, in designing a switched capacitor filter, analog to digital converter, etc. In these cases, the designs of the individual op- amps are combined with feedback and by various parameters that affect the amplifier such as input capacitance and output resistance [7]. Op amp is the back bone for many analog circuit designs [8]. It is a fundamental building block for many circuit designs that utilize its high gain, high input impedance, low output impedance, high bandwidth and fast settling time.

The speed and accuracy of these circuits depend on the bandwidth and DC gain of the op-amp. The larger the bandwidth and gain, the higher is the speed and accuracy of the amplifier[9]. A final major transitional phase op amp history began with the development of the first integrated circuit (IC) op amps, in the mid 1960s. Once IC technology became wildy established,things moved quickly through the latter of 20th years, with milestone after milestone being made in device performance[10].

1.2 Statement of the problem

The design of a single stage folded cascode is challenging, compared with the other single stage CMOS op amp topology, that is, the telescopic CMOS op amp because

the folded cascode consumes twice as much current than telescopic. However the folded cascode CMOS op amp topology is widely used due to the following basic reasons[11,12].

- the input and output stages are easily shorted
- the selection of input common mode level is easier
- voltage swing is high, etc.
- The major advantage of single stage op-amp is that it provides great stability and large phase margin[13].

1.3 Research Questions

1. How can we design and simulate a single ended output folded cascode CMOS op amp circuit?
2. How can we determine different performance parameters, like input/output voltage swing, DC open loop gain, slew rate, etc by using computer assisted simulation?

1.4 Objectives of the Study

General Objective:

The main objective of the study is to design a single ended output folded cascode CMOS op amp circuit.

Specific objectives:

1. To analyze the the single ended output folded cascode CMOS op amp circuit by using PSPICE design and simulation software.
2. To analyze various performance parameters of the single ended output folded cascode CMOS op amp circuit for device applications.
3. To increase the gain and stability of the single ended output folded cascode CMOS op amp.

1.5 Significance of the Study

Folded cascode CMOS op-amp is capable of driving a very large load with low power consumption and faster rate than two stage op-amps. This research study will help us to reduce cost and time wastage that usually occur during ordinary workshop based practices.

1.6 Scope of the Study

This thesis is based on analog electric devices and advanced single stage folded cascode design fundamentals. It requires:

- Computer simulation and
- Data analysis by using OrCAD PSPICE software

1.7 Organization of the Thesis

The thesis has been organized under five chapters:

Chapter 1: Introduction

Presents background of study, history of folded cascode CMOS op amp, PSPICE software, Statement of the problem, research questions, objective of the study, significance of the study and scope of study.

Chapter 2: Literature Review

Discusses about concepts of CMOS cascode and CMOS op amps, different topologies of CMOS op amps with their comparisons, different performance parameter of CMOS op amps.

Chapter 3: Methodology

Discusses about design methodology, procedures, specification, mathematical formulations and calculations of transistor sizes and other parameters for the proposed layout.

Chapter 4: Design and Simulation of single ended output folded cascode CMOS op amp

Describes the design, simulation and analysis of the results for the performance parameters of the proposed single ended output folded cascode CMOS op-amp circuit to achieve the research objectives.

Chapter 5: Conclusion and Recommendations

Main conclusions from the research work were drawn and possible future study areas for further improvements have been recommended.

Chapter 2

LITERATURE REVIEW

This chapter presents an over view of previous researcher works on Cascode op amp topology, as well as different CMOS op-amp topologies, and CMOS op amps . It concern on comparisons of different topologies of op-amp toward factor affecting high gain and stability. We use the following techniques to modify our input stage design from different constraints; such as input offset voltage, dynamic change, DC open loop gain, unity gain band width, common mode rejection ratio (CMMR) and slew rate are reviewed discussed at this chapter.

2.1 The Concept of Cascode Topology

The cascade of a common source stage and common gate stage is called a cascode topology, providing many useful properties [14]. The idea behind the cascode structure is to convert the input voltage to a current and apply the result to a common gate stage. In order to improve the gain of the amplifier, the designer uses the cascode structure. As we know, the input signal of a common-gate stage may be a current and also that in the common-source arrangement, the transistor converts a voltage signal to a current signal. The term cascode Stage is nothing but the combination of Common Source and Common Gate Stages. Fig.2.1 shows the basic configuration of a cascode stage:

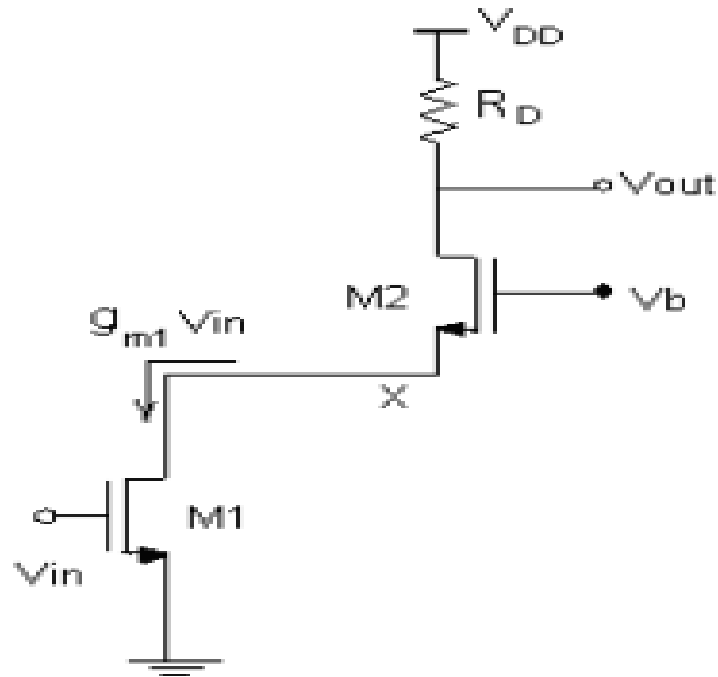


Figure 2.1: Cascode stage[15].

From the above figure, M_1 generates a small signal drain current that is proportional to V_{in} and M_2 simply routes this current to R_D . Note that in figure 2.1, M_1 and M_2 carry equal currents. As we describe the attributes of the circuit in this section, many advantages of the cascode topology over a simple Common-Source stage become evident [14, 16]. In modern circuits, the cascode is often constructed from two transistors (BJTs or FETs), with one operating as a common emitter or common source and the other as a common base or common gate. The cascode improves input output isolation (reduces reverse transmission), as there is no direct coupling from the output to input. This eliminates the Miller effect and thus contributes to a much higher bandwidth.

There are two types of cascode configurations; normal cascode and folded cascode configurations. Normal cascode is a combination of common source to common gate

stage in series configuration. One big advantage of the normal cascode configurations is that it can increase gain that depends upon the number of stages which are cascoded. The main requirement of normal cascode is that both the transistors must be same, i.e., both must be either p channel or n channel, as shown in figure 2.2 for n channel normal cascode configuration. Normal cascode has the following disadvantages: the power supply requirement is very high and the GBW product is not constant, as the gain increases with this configuration, the bandwidth decreases as a result the GBW is not constant.

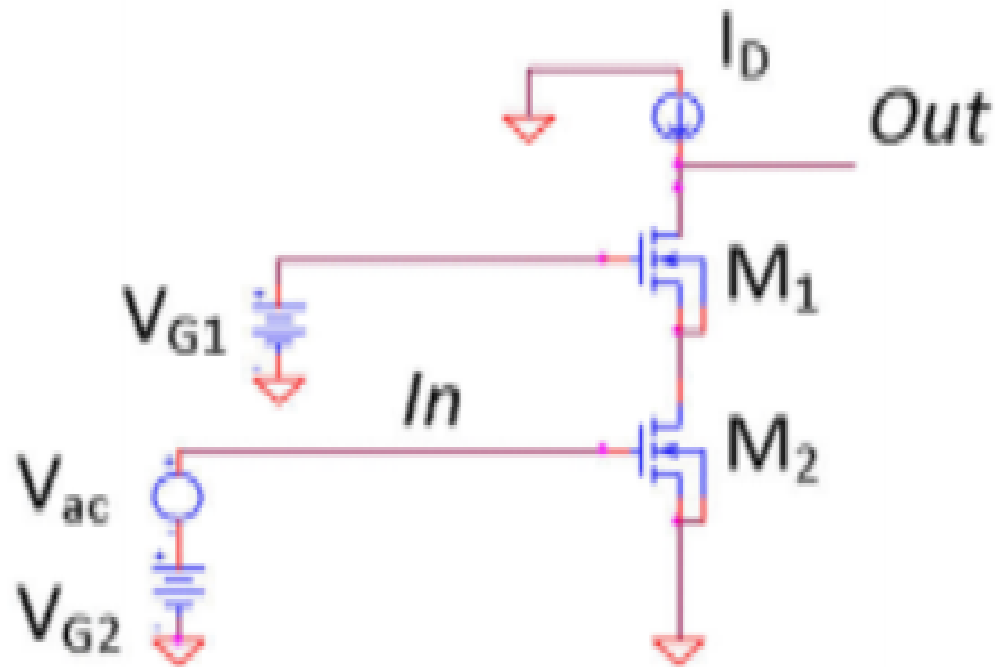


Figure 2.2: Normal Cascode Configuration

Folded cascode configuration is an extension of normal cascode configuration. The main difference is that the folded cascode consists of two transistors; either one n channel and the other p channel or both n channel transistors in a way that both

transistors must face each other [16].

2.2 CMOS Op Amp

Complementary metal oxide semiconductor (CMOS) operational amplifiers took their name from the use of MOSFETs (metal oxide semiconductor field effect transistors). MOSFETs are simpler to fabricate and therefore less expensive than BJT amplifiers, still providing a sufficiently high transconductance to allow the design of very high performance circuits. In high performance CMOS op amp circuits, transistors are not only used to amplify the signal but are also used as active loads to achieve higher gain and output swing in comparison with resistive loads. CMOS op amp has many inter-related parts, and in many ways, it is the most important building block of linear CMOS and switched-capacitor circuits. Its performance usually limits the high-frequency application and the dynamic range of the overall circuit. [5] It usually requires most of the DC power used by the device. Without a thorough understanding of the operation and the basic limitations of these amplifiers, the circuit designer can not determine or even predict the actual response of the overall system. The key advantages of CMOS op amps include extremely small input bias current (on the order of pA) and low power consumption. The CMOS process features low withstand voltage, making them suitable for low supply voltage applications. Although bipolar op amps provide higher input bias current and current consumption, they offer higher withstand voltage, low noise, low offset, and wide bandwidth.

2.3 CMOS Op-amp Topologies

Depending on a number of design issues like dynamic range, bandwidth and power consumption, the topology of op-amp has been classified broadly into two types; single-stage and two-stage op amps. Dynamic range is the ratio of the strongest to the weakest sound intensity that can be transmitted or reproduced by an audio or broadcasting system. Bandwidth is the range of frequencies within a given band, in particular that used for transmitting a signal.

2.3.1 Single Stage Op-amp

When only one transistor with associated circuitry is used for amplifying a weak signal, the circuit is known as a single stage transistor amplifier, as shown in figure 2.3.

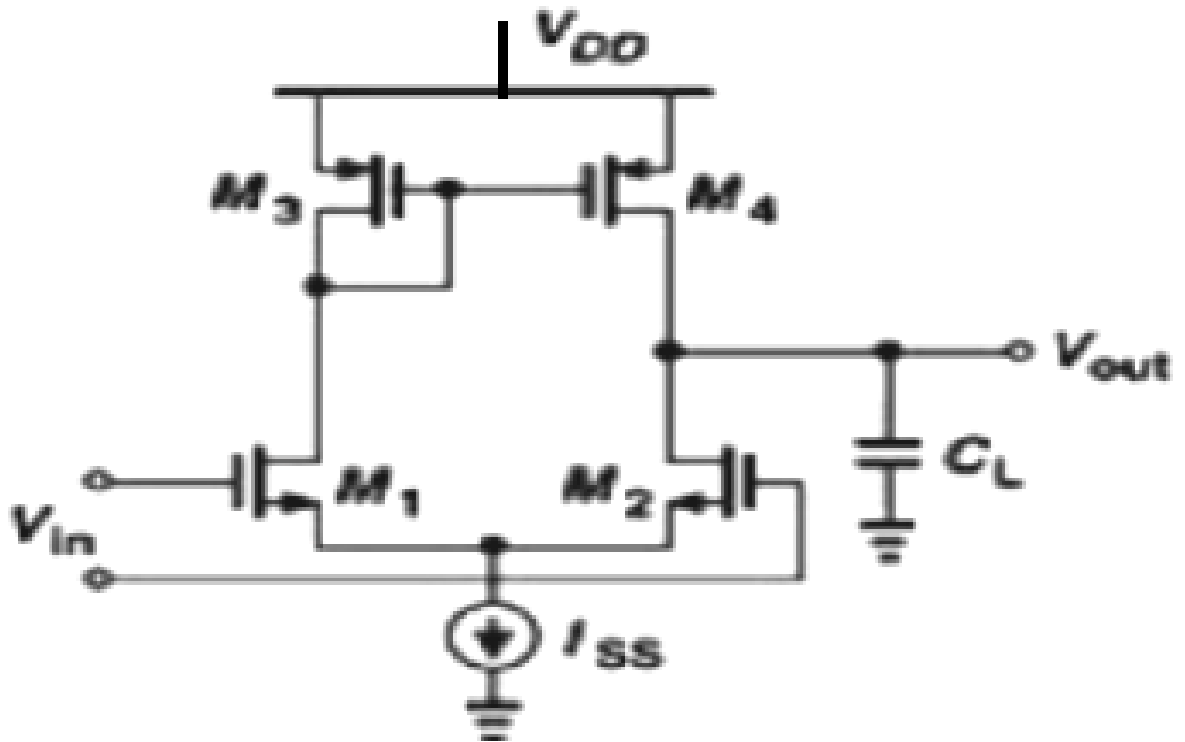


Figure 2.3: Single Stage Op-amp Topology.

This amplifier has one transistor bias circuit and other auxiliary components. Although a practical amplifier consists of a number of stages, yet such a complex circuit can be conveniently split up into separate single stages, By analyzing repeatedly, we can effectively understand the complex circuit. The analysis of a single stage amplifier is of great value in understanding the practical amplifier circuits. When a weak AC signal is given to the base of a transistor, a small base current (which is also AC) starts flowing due to transistor action (the transfers of input current signal from low-resistance circuit to a high-resistance circuit), a much larger AC current flows through the collector load R_C . Single stage topology is commonly used because of its capability of driving large capacitive load, this is due to the fact that the load capacitor acts as the compensation capacitor. Single stage architecture naturally suggests low power consumption and it is faster than multistage designs due to the presence of fewer poles and fewer current legs. But it is very difficult for a single stage circuit to meet the requirements for gain and dynamic range under very low supply voltage like that of 3V or low [17].

2.3.2 Telescopic Cascode Op-amp

In this type of CMOS topology, the cascodes are connected between the power supplies in series with the transistors in the differential pair, resulting in a structure in which the transistors in each branch are connected along straight lines, as shown in figure 2.4 [18].

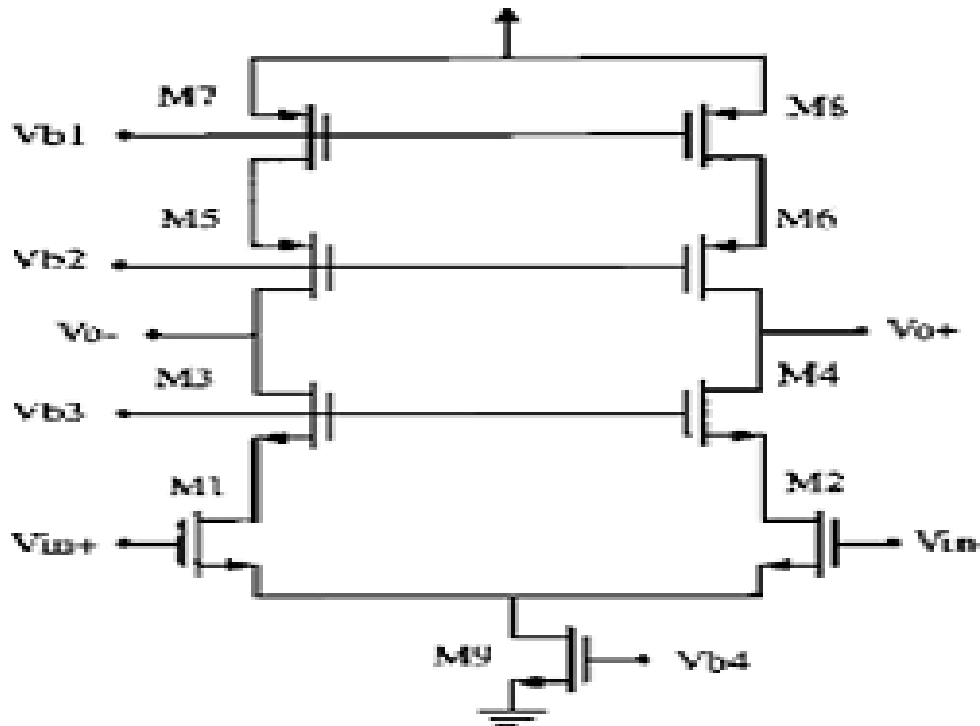


Figure 2.4: Telescopic Cascode Op-amp Topology.

This structure is smaller than that of the folded cascode because the tail transistor directly cuts into the output swing from both sides of the output. In the telescopic cascode op-amp all transistors are biased in the saturation region. Telescopic op-amp usually provides the best trade-off solution between gain, power dissipation, speed, and noise [19]. The small signal DC current gain of telescopic amplifier is more than that of the folded cascode structures. The disadvantage of a telescopic op-amp is severely limited output swing [20]. In the telescopic op amp topology:

- the input and output swing will be limited,
- the negative output swing is a function of input common mode,

apply the result to a common gate stage. Folded cascode op amp uses cascading in the output stage combined with an unusual implementation of differential amplifier to achieve ICMR. Folded cascode can be formed by two types of transistor signal paths; NMOS and PMOS types. These types of signal paths produce a different op-amp circuit performance. However, the folded cascode op-amps easily control the input and output of common mode and it can operate at a low voltage supply.

The folded cascode op amp has a push-pull output (matched transistors conducting alternately) stage which can sink or source current from the load. The exact match of the currents in the differential amplifier is not demanded by the folded cascode op amp, since extra current can flow in or out of the current mirrors. While the bias current of the conventional op amp delivers the current to both the input devices and the cascode devices as they are stacked together, the bias current (I_{BIAS}) of the folded cascode supplies only to the input devices. The folded cascode op amp has good PSRR as compared to the two stage op amp and telescopic operational amplifier [24]. Folded cascode operational amplifier topology :

- offers self-compensation,
- has good input common mode range,
- has good gain
- is easy to stabilize,
- has an output swing which is much better than telescopic, and
- has an input common mode, at least as good as the two stage amplifier.

2.3.4 Two stage CMOS Op-amp

A two-stage op-amp topology mainly consists of a cascade of voltage-to-current and current-to-voltage stages, as shown in figure 2.6.

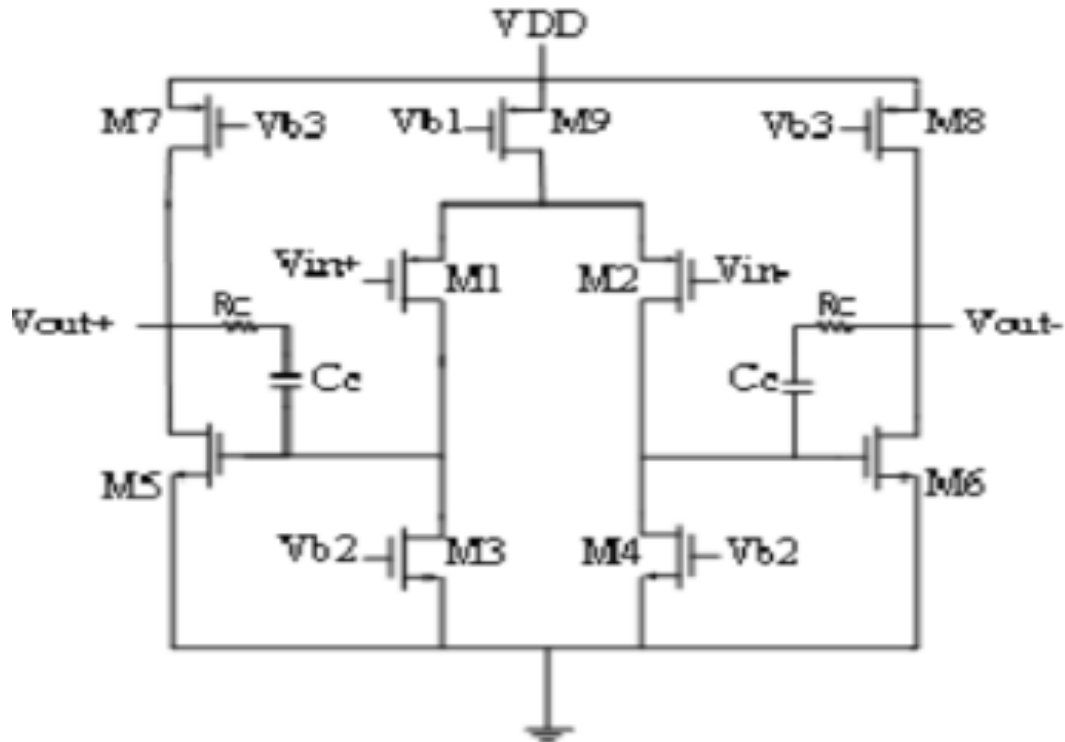


Figure 2.6: Two Stage Op-Amp Circuit Diagram.

The first stage consists of a differential amplifier converting the differential input voltage to differential currents. These differential currents are applied to a current mirror load recovering the differential voltage. The second stage consists of common source MOSFET converting the second stage input voltage to current. This transistor is loaded by a current sink load, which converts the current to voltage at the output. The second stage is also nothing more than the current sink inverter. The Two stage topology has high power consumption because of the two stages used in its design. This op-amp particularly has applications in telecommunications. After its initial success, it was noted that, this op-amp suffers from a poor PSRR[25], especially very poor negative PSRR at higher frequencies. Two-stage op-amp topology consist of an input differential stage and a second common-source stage. The differential input stage provides initial gain and this gain is increased by the second stage and hence maximizes the output. The first stage of the two-stage op amp having differential inputs converts the given input voltage to current[26]. The second common source

(CS) amplifier stage converts current to voltage. Two stage operation amplifier:

- is harder to stabilize due to two poles
- needs common technique to stabilize, which usually is done by Miller compensation capacitor.

Table 2.1 gives a summary of the performance parameters of different CMOS op amp topologies.

Table 2.1: Comparison of various Op-amp topologies

S. No.	Performance Parameters	Telescopic	folded Cascode	Two-stage
1	Gain	medium	medium	high
2	Swing	medium	high	highest
3	Speed	highest	high	low
4	Power	low	medium	medium
5	Noise	low	medium	low

As we have seen the information from Table 2.1, the folded cascode is preferable op amp topology with regard to high voltage swing and high speed with medium gain, power dissipation and noise than the other topologies. When the speed of a particular op amp is high, then the time rate of change of out put voltage called slew rate is maximum. Also, the input/output voltage swing will be maximum. Thus, if one needs maximum slew rate and input/output voltage swing, the folded cascode topology is the best candidate for selection as compared to other topologies.

2.4 Performance Parameters of CMOS Op-amps:

The best favorable selection and an optimum performance of an op-amp to be used in a particular application is often the key factor which determines the success or failure of a circuit. In this regard, power dissipation, ICMR, differential open loop gain, common mode gain, GBW, PM, CMRR, PSRR, offset voltage, input/output voltage swing, SR, are the main performance parameters to be considered during the selection process.

2.4.1 Power Dissipation:

It is the power consumed by the circuit under standby conditions. The power used in the presence of a large signal can significantly exceed the one required in quiescent conditions. Moreover, the consumed power depends on the speed specifications. Typically, higher bandwidth leads to higher power consumption. Low power operation is a very important quality factor for batteries that should supply the system for hours or days to power more and more electronic systems. In addition, low power dissipation is required by hand-held and portable devices, since it is difficult to connect to AC source in remote and rural areas. Thus, a key design task is to achieve the minimum power consumption for a given required speed. Izatul Syafina Ishak has found a typical power consumption of 0.3 mW by using $0.13\mu\text{m}$ technology with load capacitance of 1.0 pF [27]. Kyle Edward Addington has found a typical power consumption of 6.8 mW in $1.2\mu\text{m}$ Silicon Carbide (SiC) CMOS process technology with a 5 pF load capacitor[28].

2.4.2 Input Common Mode Ratio (ICMR)

The range of common mode input voltage up to which the transistors associated with the differential stage are in saturation and give a constant gain is the range of DC common mode input voltage for which the op-amp behaves normally with its key parameters, including offset voltage and input bias current. It is an important parameter when the op-amp is used in the unity gain frequency configuration. The configuration to Measure ICMR is shown in figure 2.7. [28]

Kyle Edward Addington has found an input common mode range from -0.3V to 9.25V, in a $1.2\mu\text{m}$ Silicon-Carbide CMOS process technology, using a 5pF load capacitors, as shown in the figure 2.8 [28].

2.4.3 Open Loop Gain

DC open loop gain is the gain an amplifier at different frequencies of the input AC signal. It is the gain obtained when no feedback is used in the circuit. Open loop gain is usually exceedingly high. In fact, an ideal operational amplifier has infinite open-loop gain. However a very high gain of the operational amplifier enables considerable levels of feedback to be applied to achieve a given required performance. The open loop gain of an operational amplifier falls very rapidly with increasing frequency.

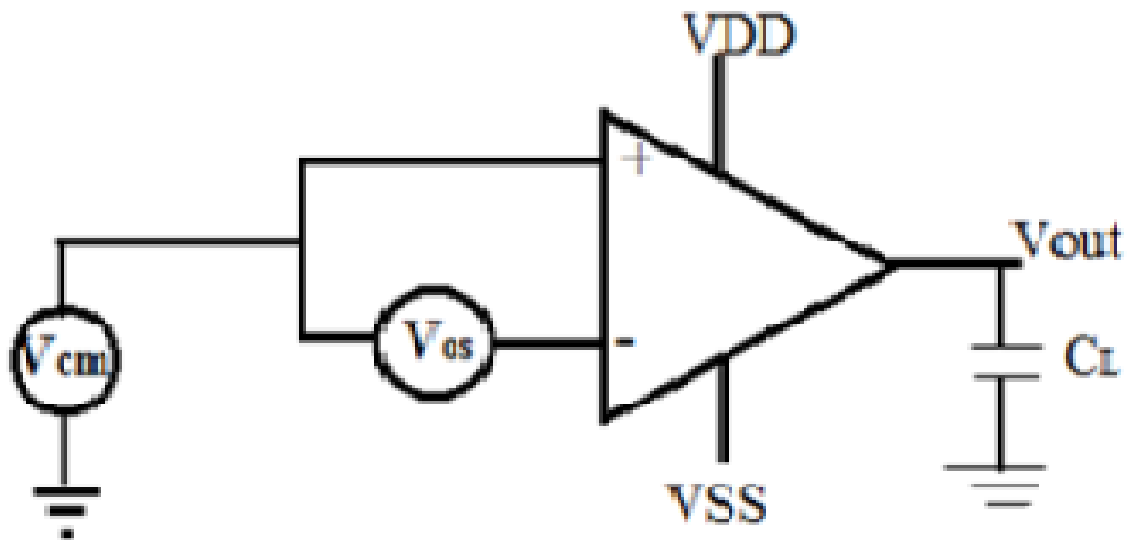


Figure 2.7: The Configuration to Measure ICMR [28].

Along with slew rate, this is one of the reasons why operational amplifiers have limited bandwidth. The gain is measured using DC operating point. The circuit configuration to measure the DC open loop gain is shown in figure 2.9 (a) [27]. By using $0.13\mu\text{m}$ technology, Izatul Syafina Ishak has obtained an open loop DC gain of 64.5dB as shown in figure 2.9 (b)[27].

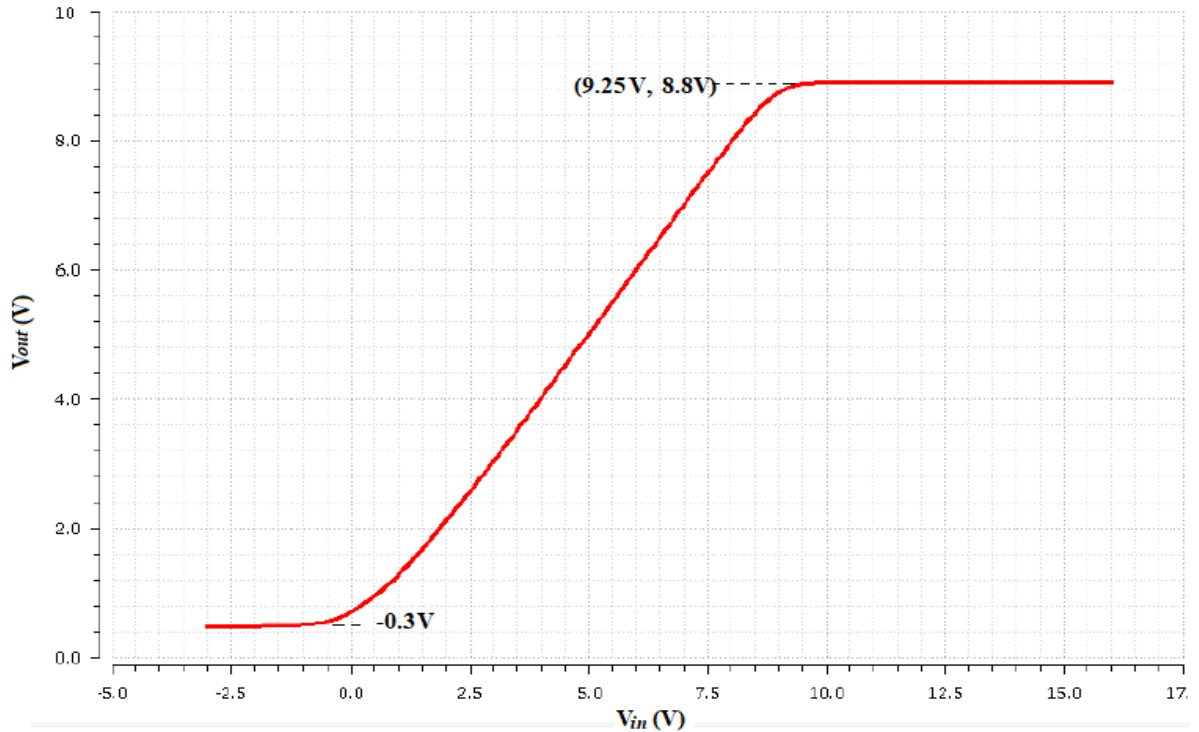


Figure 2.8: ICMR Simulation Result obtained by Kyle E. Addington [28].

2.4.4 Phase Margin (PM) and Gain bandwidth (GBW)

The phase shift of the small signal differential gain measured at the unity gain frequency is called phase margin. In order to ensure stability when using the unity gain configuration, it is necessary to achieve a phase margin better than 60. A lower phase margin like 45 will cause ringing in the output response. GBW is defined as the frequency range over which the amplifier voltage gain is greater than 70.7 or -3dB (where we consider the maximum gain to be the reference or 0dB) of the maximum output value attained by the gain of the amplifier. The frequency at which the gain becomes 0dB is called unity gain frequency (f_{unity}) or gain bandwidth. [27 - 29] From figure 2.9 (b), one can observe that the value of the phase margin done by Izatul Syafina Ishak exhibits 68.4° with the unity gain bandwidth (UGB) at 133.1MHz, by using $0.13\mu\text{m}$ a technology. [27]

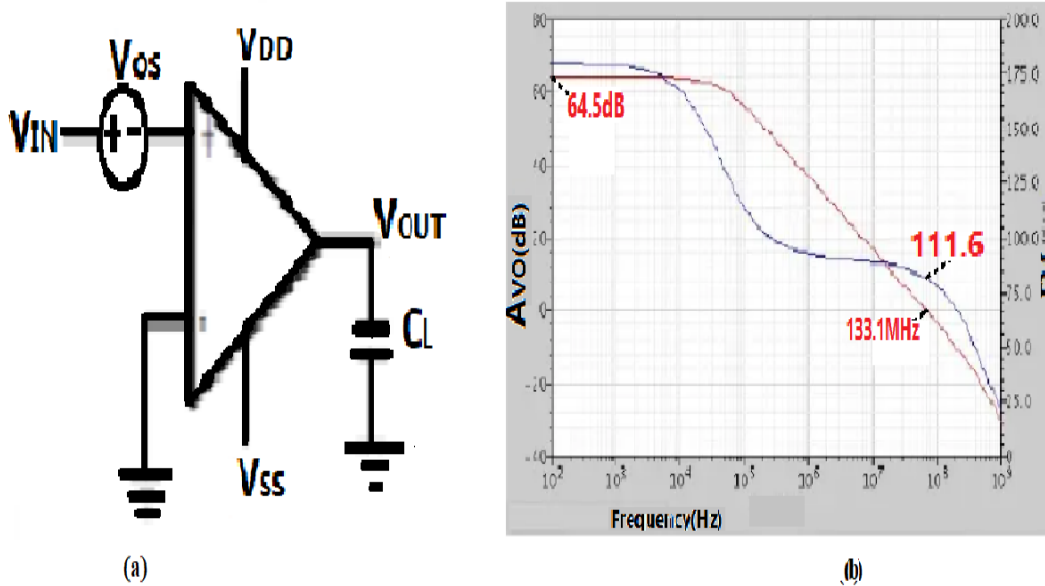


Figure 2.9: a) Configuration to measure the open loop gain. (b) Simulation Result of Open Loop Gain obtained by Izatul Syafina Ishak [27].

From figure 2.10 (a), one can also observe that Kyle Edward Addington, has obtained an open loop DC gain of 50.0dB, a phase margin of 51.523° and unity gain bandwidth of 2.6MHz in $1.2\mu\text{m}$ Silicon Carbide (SiC) process technology, with a 5 pF load capacitor. [28] From figure 2.10 (b), one can see that Zhang Kun, et al. have obtained an open loop DC gain of 95.29dB, a phase margin of 83.5° and unity gain bandwidth of 7.479MHz, by using $0.18\mu\text{m}$ SMIC CMOS technique[29].

2.4.5 Common mode rejection ratio(CMRR)

The measure of an amplifiers ability to reject common-mode unwanted signals appearing with the same polarity on both input lines. The CMRR is the ratio of the differential voltage gain to the common-mode voltage gain. CMRR falls off as the frequency increases.

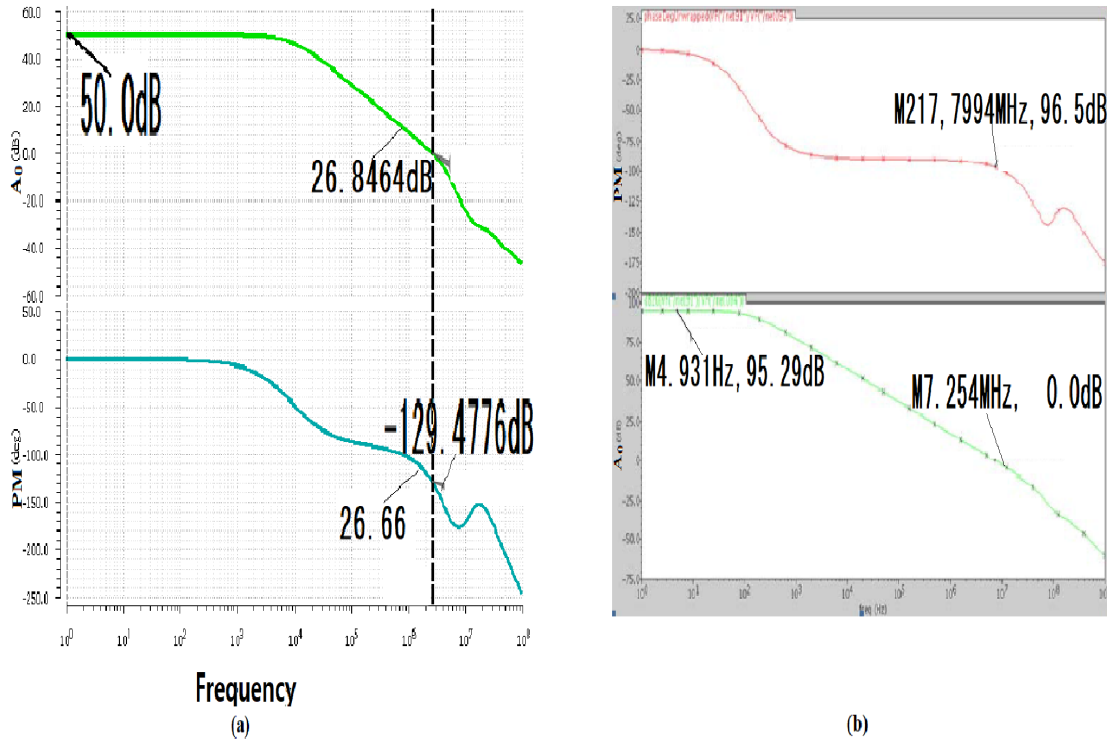


Figure 2.10: Simulation Result of Phase Margin and Gain Bandwidth obtained by a) Kyle Edward Addington [28].; b) Zhang Kun, et al [29].

Mathematically, the CMRR is defined as:

$$CMRR = \frac{A_{DM}}{A_{CM}} \tag{2.4.1}$$

The value of CMRR can be computed in logarithmic scale so as to convert it into decibel form. Mathematically it is expressed as;

$$CMRR(in\ dB) = 20 \times \log \frac{A_{DM}}{A_{CM}} \tag{2.4.2}$$

Izatul Syafina Ishak has found a typical common mode rejection ration of 41.48 dB, as shown in figure 2.11 [27].

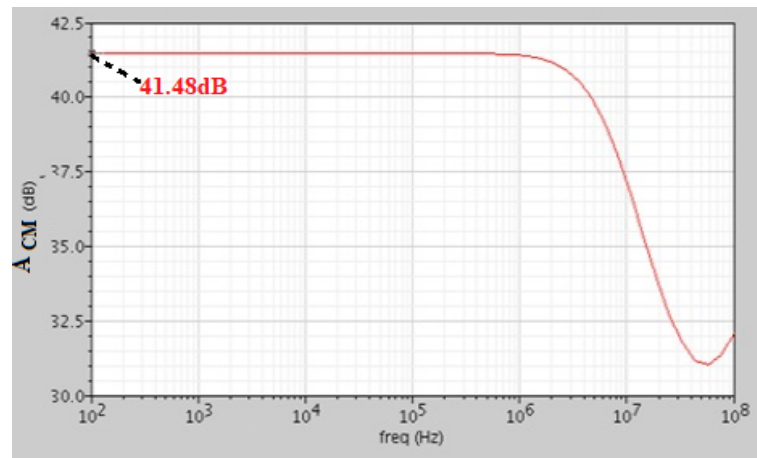


Figure 2.11: Simulation Result of CMRR obtained by Izatul Syafina Ishak [27].

2.4.6 Power Supply Rejection Ratio (PSRR)

PSRR is defined as the ratio of the output voltage to the change in the power supply caused by a small AC input signal in an open loop mode. PSRR has two merit factors showing the ability of the op amp to reject spur signals coming from the power supply. Having a good PSRR is an important merit. If we apply a small AC signal in series with the positive or the negative power supply, we obtain a corresponding signal at the output with a given amplification.

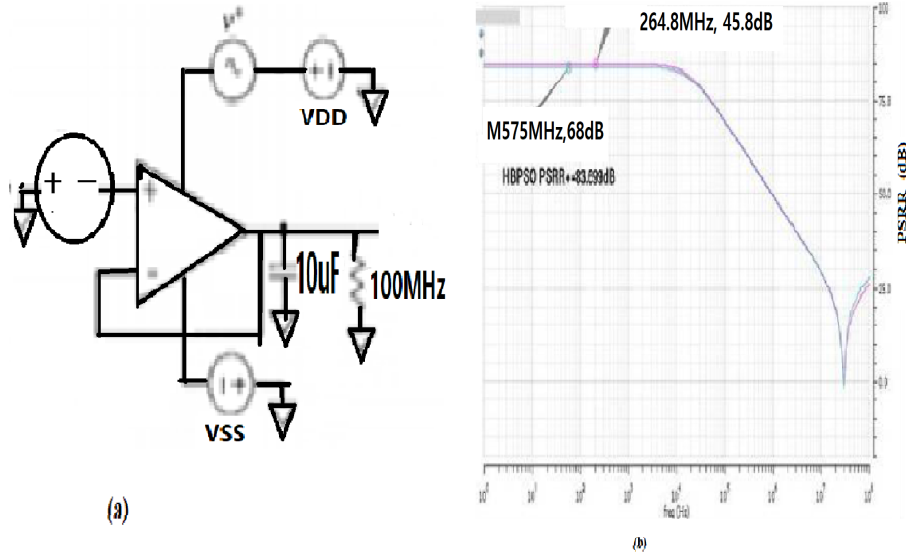


Figure 2.12: a) Configuration to Measure PSRR, [27-29] b) Simulation Result of PSRR obtained by P. K. Paul, et. al[30].

P. K. Paul, et. al. have found typical power supply rejection ratio values of 84.5431dB and 83 699dB, using two methods [30]. Also, Er. Rajni has found a typical power supply rejection ratio of 55 dB [31].

2.4.7 Input/output voltage swing

It is defined relative to the power supplies; the range of input voltages that allow for linear operation of output signals. The output signal becomes distorted and non-linear if it one exceeds the op amp output swing specifications. The output voltage swing range, the response of the op-amp, should conform to the given specification and in particular the harmonic distortion should remain below the required level. Figure 2.13 shows the configuration to measure output voltage swing.

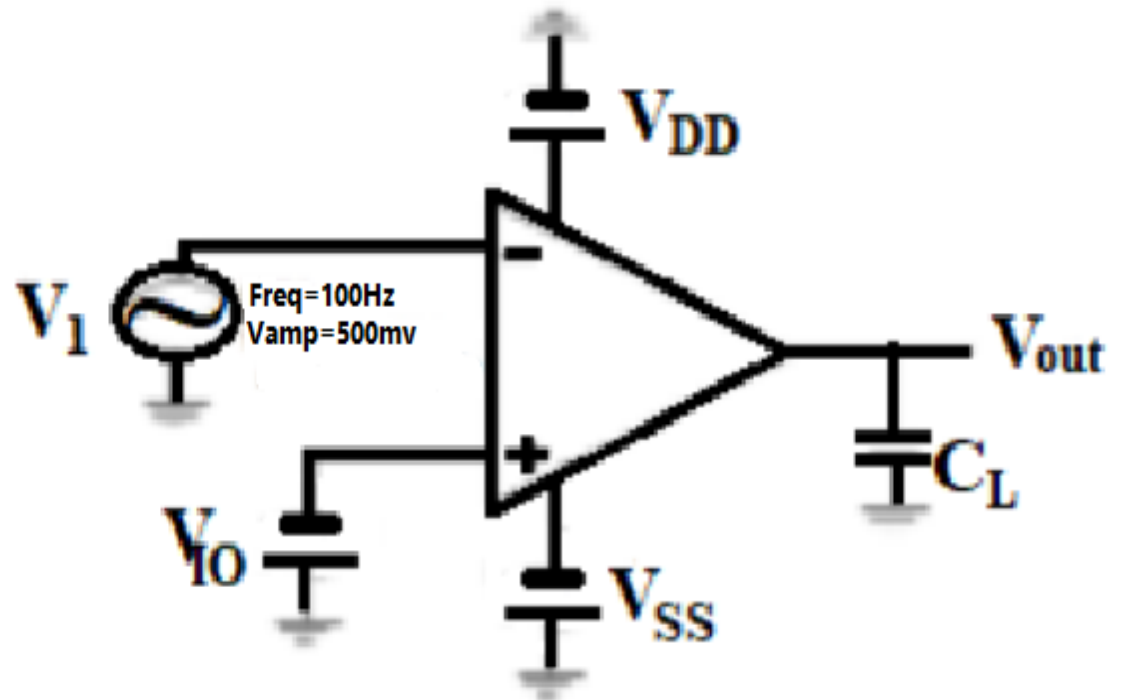


Figure 2.13: The configuration to measure the voltage swing [27, 28]

Kyle E. Addington has found $V_{O(max)} = 7708.767$ mV and $V_{O(min)} = -7189.471$ mV, as shown in figure 2.14 [28]. These peak-to-peak output voltages represent the maximum output voltage swings. When the output voltage exceeds this range, the wave obtained will experience clipping.

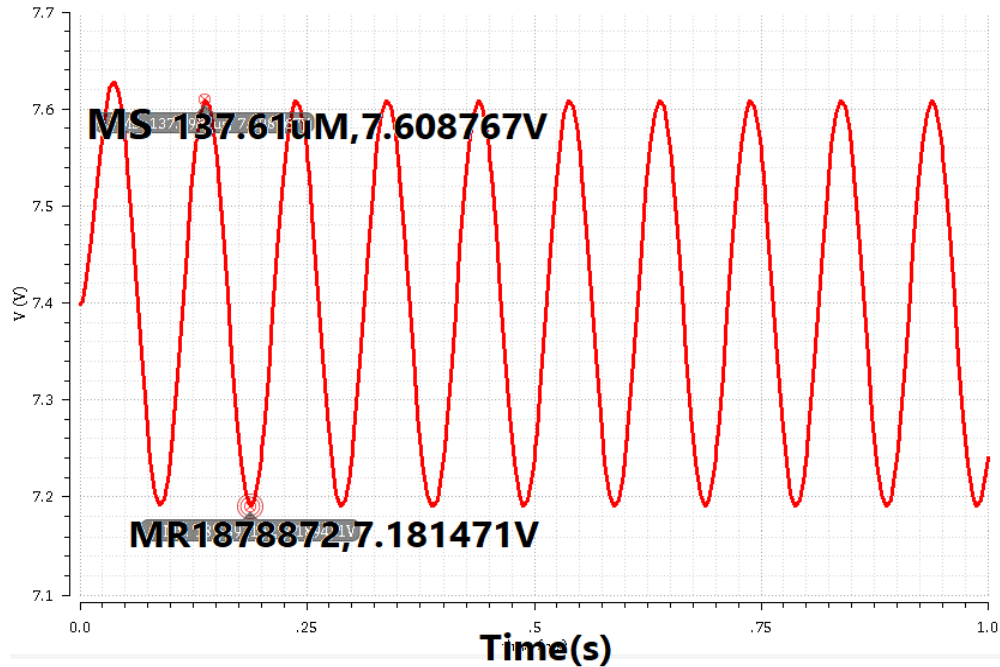


Figure 2.14: Simulation result of voltage swing obtained by Kyle E. Addington [28].

2.4.8 Slew Rate(SR)

SR is the maximum achievable time derivative of the output voltage[26, 27]. It is measured using the op-amp in the unity gain configuration, as shown in Figure 2.15. A large input step voltage fully imbalances the input differential stage and brings the op-amp output response into the slewing conditions.

Mathematically, it can be expressed as:

$$SR = \left. \frac{dV_{out}}{dt} \right|_{Max} \quad (2.4.3)$$

A transient analysis was performed by obtaining the rate of change of output with time. For example, as illustrated in figure 16, for the rising edge, the slew rate has been found to be $22.6 \text{ V}/\mu\text{s}$ as done by Izatul Syafina Ishak [28].

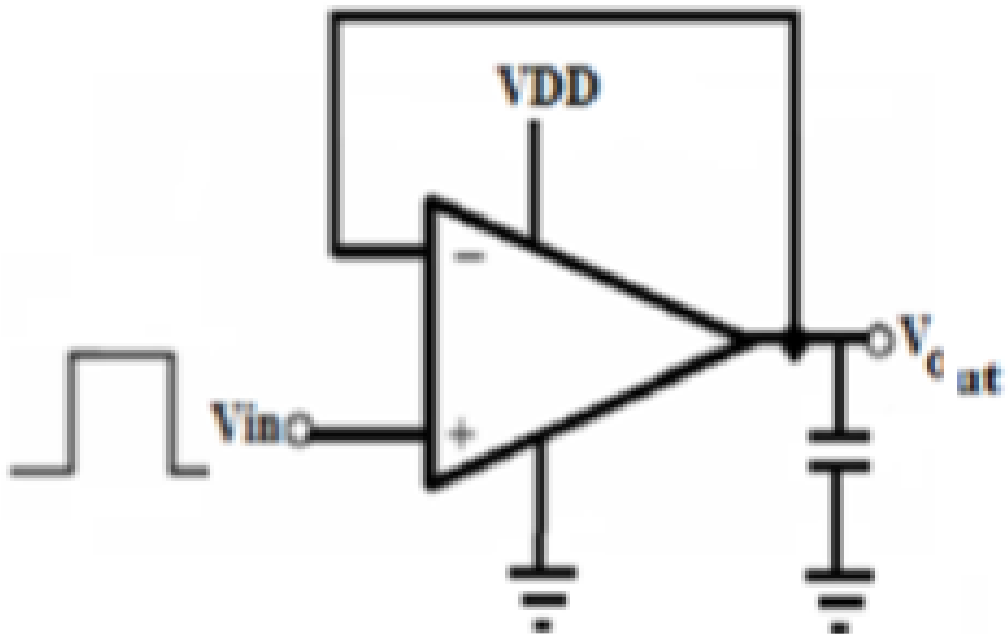


Figure 2.15: Configuration to Measure Slew Rate [27].

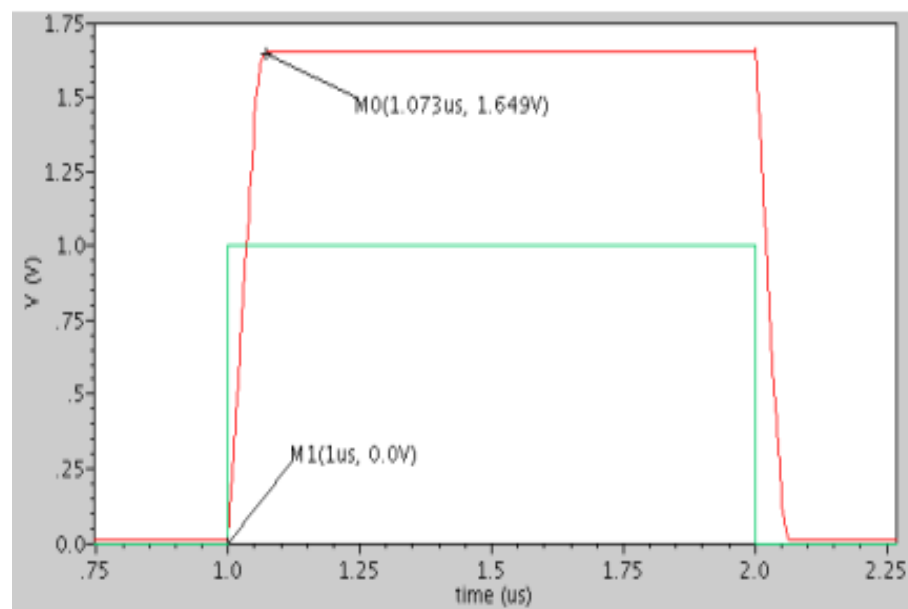


Figure 2.16: Simulation result of slew rate obtained by Izatul Syafina Ishak [28].

Chapter 3

METHODOLOGY

3.1 Design, Methodology and Schematic Layout

This chapter will describe the topology selection, device performance parameter specifications and the procedure to be followed during design and simulation of single ended output folded cascode CMOS op-amp proposed in our Thesis work. The design flow of the folded cascode CMOS operational amplifier includes defining the requirements of the amplifier, defining the process design, selecting the layout, stating the target inputs and outputs, hand calculations, computer assisted simulations, and finally fine tuning the circuit for optimal device performance. The design procedure assumes that, the open loop DC gain (A_{DM}), unity -gain bandwidth (GBW), input common-mode range ICMR [$V_{in(min)}$ and $V_{in(max)}$], load capacitance (C_L), Slew rate (SR) and Power dissipation (P_D) are given.

The single ended output folded cascode CMOS op amp circuit proposed in our research is shown in figure 3.1. The layout consists of 10 transistors out of which four, that is, M_1 , M_2 , M_3 and M_4 are PMOS and the remaining six M_5 , M_6 , M_7 , M_8 , M_9 and M_{10} are NMOS transistors. The differential input stage is made from M_9 and M_{10} , which are folded down. M_1 to M_8 form the cascode configuration. The circuit is supplied by a single source, $V_{DD} = 2.5V$. The cascode structure is generated by a low-voltage cascode that works by connecting the nodes as stated as V_{b1} and V_{b2} to DC bias voltages. The function of the 5 pF capacitor load in this circuit is to stabilize the phase that is produced by the op-amp circuit. The gate of M_9 is inverting and that of M_{10} is noninverting input of the circuit respectively. In most CMOS technologies the number of PMOS transistor are lower than NMOS transistors, because

the mobility of holes (μ_p) is lower than the mobility of electrons (μ_n) with a ratio of $0.25 \mu_p C_{ox}$ to $0.75 \mu_p C_{ox}$.

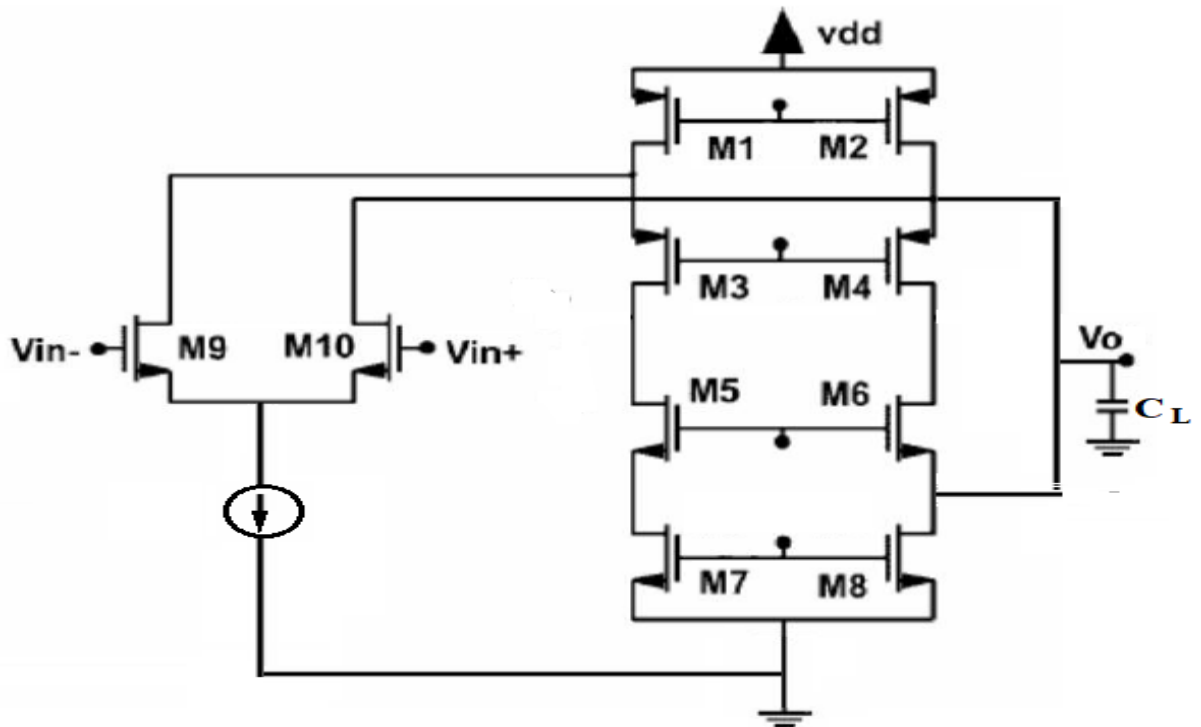


Figure 3.1: Schematic Lay out of Single-Ended Output Folded Cascode CMOS Op amp.

3.2 Design Specifications and Boundary Conditions

In this study we will design a single ended output folded cascode CMOS op amp circuit that meets the specification listed in Table 3.1 and the boundary conditions listed in Table 3.2.

Table 3.1: Specification for Folded Cascode CMOS op-amp. [28, 29]

S.No.	Parameters	Proposed value
1	supply voltage	± 2.4
2	GBW	$\geq 9.8MHz$
3	CMRR	$50dB$
4	ICMR	$-2.4V$ to $2.4V$
5	Load Capacitance (C_L)	$10pF$
6	SR	$6V/\mu s$
7	Technology	$0.3\mu m$
8	DC gain (A_{DM})	$\geq 50dB$
9	power dissipation (P_D)	$5mW$
10	PM	$\geq 45^\circ$
11	Bias current	$11\mu A$

Table 3.2: Values of Boundary conditions

S.No.	Boundary Condition	Requirement
1	$\mu_P C_{ox} = K_P$	$40\mu AV^{-2}$
2	$\mu_N C_{ox} = K_N$	$80\mu AV^{-2}$
3	$V_{TH,P}$	$-0.66V$
4	$V_{TH,N}$	$0.66V$
5	λ_n	$0.06V^{-1}$
6	λ_p	$0.05V^{-1}$
7	$V_{T3(MAX)}$	$0.74V$
8	$V_{T3(MIN)}$	$0.63V$
9	V_{GS}	$0.82V$

3.3 Design Procedure

The design procedure involves the following sequence of steps.

- Selecting a specific topology,
- Determining the DC current, and
- Calculating the aspect ratio (W/L) of each transistor.

To determine the W/L ratio of each of the ten transistors could be determined in two ways; by using either the gain requirements or the input and output range requirements. Both the requirements are dependent upon overdrive voltage (V_{ov}) and the transconductance (gm). By selecting the desired gm or V_{ov} and using equations(3.3.1) and (3.3.2) with the required bias current, the appropriate W/L ratios can be calculated.

$$I_D = \frac{1}{2} \times K' \left(\frac{W}{L} \right) V_{ov}^2 \quad (3.3.1)$$

$$gm = K' \left(\frac{W}{L} \right) V_{ov} \quad (3.3.2)$$

Since the input range and output range equations are typically simpler, it is preferred to use those specifications to design the W/L, and then return afterwards to make sure the gain requirements are met. If after calculating the W/L ratios for the input and output range, the gain and phase margin requirements are not met, there are some modifications that the designer can make. To increase the gain of the circuit, the size of the input differential pair transistors can be increased. This will increase the gain of the circuit, but also decreases the phase margin of the circuit. In order to increase the phase margin of the circuit, a compensation capacitor can be placed at the output node of the amplifier. The increased capacitance will improve the phase margin, however, this will trade away some of the bandwidths. Also, the increased capacitance at the output will affect the slew rate of the amplifier. To correct the slew rate degradation, the designer can increase the current, which will speed up the circuit but increase power dissipation.

If the option to change the currents is chosen the designer must iterate back through the first stages of the design again and resize some of the transistors. Another thing that could be done is to trade off some of the input/output range for more gain by decreasing the size of the current mirror transistors, thus increasing the output resistance of the circuit. Using these design parameters all of the major specifications can be juggled and shifted until the proper balance is found[28].

♠ Bias Current (I_{BIAS})

The first step of the design gives the estimation of the bias current. Starting with the slew rate, we have

$$I_{BIAS} = SR \times C_L \quad (3.3.3)$$

To design the tail transistor M_9 and calculate its aspect ratio $(W/L)_9$, the following equation can be applied:

$$I_{BIAS} = 2I_{D9} = \frac{(\mu_n C_{ox})}{2} \left(\frac{W}{L} \right)_9 (V_{GS9} - V_{THn})^2 \quad (3.3.4)$$

♠ DC Open loop gain

The DC open loop gain of the operational amplifier is given by:

$$A_V = A_{V9i} \times A_{V10i} \quad (3.3.5)$$

where A_{V9i} and A_{V10i} are the gain of the i^{th} transistor op amp at the first and second stages, respectively. It can be formulated as,

$$A_{V9i} = G_{m9i} \times R_{out9i} \quad (3.3.6)$$

$$A_{V10i} = G_{m10i} \times R_{out10i} \quad (3.3.7)$$

where G_{m9i} and G_{m10i} are the transconductance of the i^{th} transistor in the input network and R_{out9i} and R_{out10i} are the effective output resistances of the i^{th} transistor in the output network.

The saturation region current expression helps us in calculating the aspect ratios (W/L) of transistors as the current through them is known and overdrive voltage is assigned.

$$I_D = \left(\frac{1}{2}\right) \mu_{n,p} C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{Tnp})^2 (1 + \lambda_{n,p} V_{DS}) \quad (3.3.8)$$

where I_D is drain current, $\mu_{n,p}$ and C_{ox} are mobility of carriers and oxide capacitance, respectively; V_{GS} is gate-to-source voltage, and V_{TH} is the threshold voltage.

The over all gain (A_v) of folded cascode architecture is given by:

$$A_V = G_{m9}[G_{m3}, r_{o3} \cdot (r_{o9})][r_{o1}][G_{m5} \cdot r_{o5} \cdot r_{o7}] \quad (3.3.9)$$

When the drain-source voltage is increased, the drain current I_D is obtained from ro:

$$r_o = \frac{1}{\lambda \times I_D} = \frac{V_A}{I_D} \quad (3.3.10)$$

♠ Unity Gain frequency (UGB):

Unity gain frequency is the frequency where the voltage gain of an op amp is unity. It indicates the highest usable frequency and is important because, it is equals to the gain bandwidth product.

♠ Input Common Mode Range (ICMR):

ICMR represents the voltage in the input stage range under normal operating range. That is,

$$ICMR_{max} = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T_{o3}(max)}| + V_{T_{1}(max)} \quad (3.3.11)$$

$$ICMR_{min} = V_{SS} - \sqrt{\frac{I_5}{\beta_3}} + |V_{T_{1}(max)}| + V_{DS5(SAT)} \quad (3.3.12)$$

$$ICMR = V_{DD} - V_{GS} - V_{DS} \quad (3.3.13)$$

♠ **Slew Rate (SR):**

The expression for SR is given by:

$$SR = \frac{dV_{OUT}}{dt} \quad (3.3.14)$$

Since the charge on the capacitor (Q_{CL}) is:

$$Q_{CL} = C_L \times V_{out} \quad (3.3.15)$$

$$V_{out} = \frac{Q_{CL}}{C_L} \quad (3.3.16)$$

And, current is defined by:

$$I_{CL} = \frac{dQ_{CL}}{dt} \quad (3.3.17)$$

Then, substituting equations(3.4.14) and(3.3.15) into equation(3.3.12) we obtain:

$$SR = \frac{I_{CL}}{C_L} \quad (3.3.18)$$

Now, determine the sizes of the differential input pair of the circuit (M_9 and M_{10}), by assuming both of them to be working in saturation mode. Their aspect ratios could be calculated using the bias current

$$\left(\frac{W}{L}\right)_{9,10} = \frac{I_{BIAS}}{n(V_{GS9} - V_{THP})^2} \quad (3.3.19)$$

♠ **Gain Bandwidth(GBW):**

To achieve the desired GBW, we use,

$$g_{m9} = g_{m10} = GBW \times 2\pi C_L \quad (3.3.20)$$

$$g_{mn} = \sqrt{2\mu_n C_{OX} I_{D9} (W/L)_n} \quad (3.3.21)$$

where μ_n is electron mobility in the NMOS channel, C_{OX} is gate-oxide capacitance per unit area, $(W/L)_9$ is the aspect ratio of transistor M_9 .

♠ **Effective Voltage (V_{eff}):**

The effective overdrive voltage, $V_{eff9} = (V_{GS9} - V_{THP})$, given by:

$$V_{eff9} = (V_{GS9} - V_{THn}) = \sqrt{\frac{2I_{D9}}{\mu_n C_{OX} (W/L)_9}} \quad (3.3.22)$$

♠ **Output Voltage Swing:**

The output swing represents the range of the output voltage when all the transistor operated in the active region which can be expressed as:

$$V_{out}^{(+)} = |V_{DSAT5}| = \sqrt{\frac{2I_{D5}}{K_n \left(\frac{W}{L}\right)_5}} \quad (3.3.23)$$

And

$$V_{out}^{(-)} = |V_{DSAT6}| = \sqrt{\frac{2I_{D6}}{K_n \left(\frac{W}{L}\right)_6}} \quad (3.3.24)$$

$$V_{(out)Swing} = 2(V_{DD} + V_{SS} - |V_{out6}| - |V_{out5}|) \quad (3.3.25)$$

♠ **Power Dissipation (PD):**

For a given supply voltage, we can find the total power dissipation by using [28,30]:

$$P_D = (V_{DD} - V_{SS})(I_3 + I_{10} + I_{BIAS}) \quad (3.3.26)$$

3.4 Mathematical Formulations

3.4.1 DC Analysis

DC analysis consists of bias point and DC sweep. Bias point includes node voltage, node current, and power dissipation. DC sweep is used to obtain the ICMR. Figure 3.2 shows the hierarchy for DC analysis.

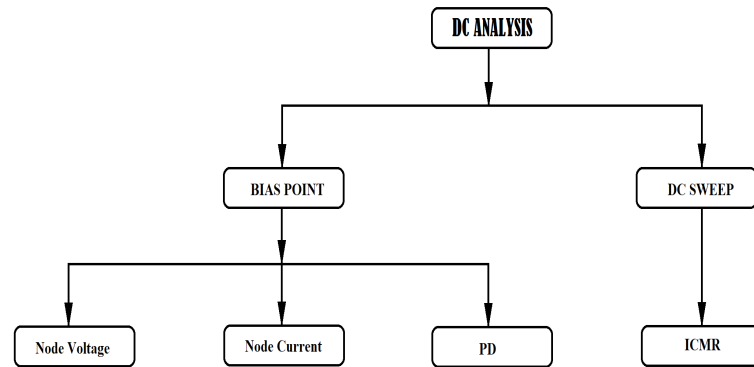


Figure 3.2: The Hierarchy for DC Analysis

3.4.2 AC Analysis

AC analysis includes AC sweep/Noise and Time domain/transient analysis. In this research, the AC sweep/noise analysis includes CMRR and DC open loop gain, while the transient analysis consists of SR and voltage swing, as shown in Figure 3.3.

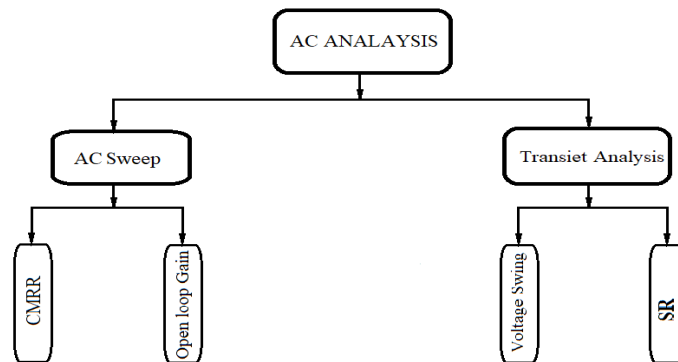


Figure 3.3: The Hierarchy for AC Analysis

3.5 Calculations of Transistor Sizes:

Determine the current through M_9 from the specification of SR :

$$I_{D9} = \frac{I_{BIAS}}{2} = \frac{I_{BIAS}}{2} = \frac{11\mu A}{2} = 5.5\mu A = I_{D10} \quad (3.5.1)$$

The current through M_1 and M_2 :

$$I_{D1} = I_{D9} = 5.5\mu A; \text{ and } I_{D2} = I_{D10} = 5.5\mu A \quad (3.5.2)$$

In turn, the current through M_3 and M_4 :

$$I_{D3} = I_{D1} = 5.5\mu A; \text{ and } I_{D4} = I_{D2} = 5.5\mu A \quad (3.5.3)$$

The above current values ensure that M_1, M_2, M_3, M_4, M_9 and M_{10} are in saturation. Whereas, the rest transistors, that is, M_5, M_6, M_7 and M_8 , remain cut-off. So,

$$I_{D5} = I_{D6} = I_{D7} = I_{D8} = 0A \quad (3.5.4)$$

Calculate transistor size of M_5

$$I_{D5} = \left(\frac{1}{2}\right) \mu_p C_{OX} \left(\frac{W}{L}\right)_5 (V_{GS5} - V_{THP}) \quad (3.5.5)$$

Calculate $(W/L)_5$ from the minimum input voltage. First, calculate $D_{S5(SAT)}$, then find the aspect ratio $(W/L)_5$

$$ICMR(min) = V_{DSAT} + (V_{GS1} - V_{DD}) = (V_{GS} - V_{THP})_5 + (V_{GS1} - V_{DD}) \quad (3.5.6)$$

$$-2.4V = (V_{GS} - V_{THP})_5 + (-0.14V - 2.12V),$$

$$\text{But, } (V_{GS} - V_{THP})_5 = 0.14V \quad (3.5.7)$$

$$\Rightarrow \left(\frac{W}{L}\right)_{9,10} = \frac{2 \times I_{D5}}{\mu_p C_{OX}} (V_{GS5} - V_{THP})^2 \left(\frac{2 \times 60}{40 \times (0.14)^2}\right) = 1.53$$

Calculate the aspect ratios of the differential input pair of the circuit (M_1 and M_2) to achieve desired GBW, using the equation:

$$g_{m1} = g_{m2} = GBW \times 2\pi = 6.8 \times 10^{-6} Hz \times 6.28 \times (10)^{-12} \quad (3.5.8)$$

$$f = 46.97\mu_s \quad (3.5.9)$$

$$\Rightarrow \left(\frac{W}{L}\right)_{1,2} = \frac{(g_{m1})^2}{2 \times \mu_p C_{OX}} = \frac{(46.97)^2}{2 \times 40} = 27.5$$

Calculate $ICMR_{(min)}$ by:

$$V_{cm,in} \geq V_{(SAT)5} + V_{(GS)1} \quad (3.5.10)$$

$$V_{cm,in} \geq 0.14V + 0.14V \geq 0.28V \quad (3.5.11)$$

Calculate the width of M_3 and M_4 is obtained by using $ICMR_{(max)}$:

$$ICMR_{max} = V_{DD} - (V_{GS} - V_{TH})_4 \quad (3.5.12)$$

$$But = (V_{GS} - V_{TH})_4 = 2.4 - 2.12 = 0.28 \quad (3.5.13)$$

$$\left(\frac{W}{L}\right)_{3,4} = \frac{2I_{D4}}{\mu_p C_{OX} |V_{GS} - V_{TH}|^2}$$

$$\Rightarrow \left(\frac{W}{L}\right)_{3,4} = \frac{2 \times 0.3}{80 \times (0.28)^2} = 0.2 \quad (3.5.14)$$

Determine $(W/L)_6$ and I_{D6} by letting the second pole (P2) equal to 2.2 GBW.

$$g_{m6} = 2.2g_{m2} \times \left(\frac{C_L}{C_C}\right) \quad (3.5.15)$$

$$\Rightarrow g_{m6} = 2.2 \times 8.4 \times 18.48\mu_s = 166\mu_s$$

$$gm4 = \sqrt{2\mu_n C_{OX} \left(\frac{W}{L}\right)_4}$$

$$\Rightarrow gm4 = \sqrt{2 \times 80 \times 3.3 \times 1.05} = 23.5\mu_s \quad (3.5.16)$$

$$\left(\frac{W}{L}\right)_{5,6} = \left(\frac{W}{L}\right)_4 \times \left(\frac{g_{m6}}{g_{m4}}\right) \quad (3.5.17)$$

$$\Rightarrow \left(\frac{W}{L}\right)_{5,6} = 0.2 \times \frac{166}{23.5} = 1.42$$

$$I_{D6} = \frac{(gm6)^2}{2\mu_n C_{OX} \left(\frac{W}{L}\right)_6} \quad (3.5.18)$$

$$\Rightarrow I_{D6} = \frac{(18.48)^2}{2 \times 80 \times 1.42} = 1.5\mu_s$$

$$\left(\frac{W}{L}\right)_{7,8} = \left(\frac{W}{L}\right)_5 \left(\frac{I_{D6}}{I_{D5}}\right) \quad (3.5.19)$$

$$\Rightarrow \left(\frac{W}{L}\right)_{7,8} = 1.53 \times \frac{1.5}{0.6} = 3.75$$

The output voltage swing is calculated as follow:

$$V_{outswing} = V_{DD} - |V_{out6}| - |V_{out7}| \quad (3.5.20)$$

$$\Rightarrow V_{outswing} = 2.4 + -0.14 - .015 = 2.11V$$

The power dissipation of circuit by using:

$$P_D = (2I_{D5} + I_{D6})(V_{DD}) \quad (3.5.21)$$

$$\Rightarrow P_D = (26.6 + 10.7)(2.4+) = 106.6\mu W$$

Table 3.3: Summary of calculated values of aspect ratios (W/L).

S.No.	Transistor	Aspect ratio
1	M_1, M_2	$2.5\mu m/0.3\mu m$
2	M_3, M_4	$0.315\mu m/0.3\mu m$
4	M_5, M_6	$2.226\mu m/0.3\mu m$
5	M_7, M_8	$1.227\mu m/0.3\mu m$
3	M_9, M_{10}	$4.62\mu m/0.3\mu m$

Chapter 4

DESIGN AND SIMULATION

4.1 Circuit Design

We have designed the single ended output folded cascode CMOS op-amp circuit proposed in this Thesis, as shown in figure 4.1, based on the schematic layout given in figure 3.1. The equations used in the transistor size calculations of Chapter 3, however, give only approximate values for the parameters and are based on silicon transistors. Using a simulator with silicon-carbide based transistor models provide a much more accurate description of the circuit behavior, therefore, a second pass of the transistor sizing was performed using the Cadence OrCAD design and simulation software and the PSPICE simulator.

In Figure 4.1, the device sizes and their inter connections are shown. We have used a single-supply voltage of 2.5V. The single-ended output folded cascode CMOS op-amp circuit design process consists of defining circuit inputs and outputs, hand calculations and computer assisted parametric simulations. Parametric analysis and all transistor sizes were adjusted to achieve optimized performance. Computer assisted circuit simulation is important to fine tune the initial design given in the form of specifications and hand calculations based on appropriate equations. Using the silicon-carbide based PSPICE simulator, the aspect ratios of the topology were determined to achieve the required performance parameters of the design.

Computer assisted circuit simulation is important to fine tune the initial design given in the form of specifications and hand calculations based on appropriate equations.

The modified design with values appearing best for the proposed CMOS op amp design is shown in figure 4.1.

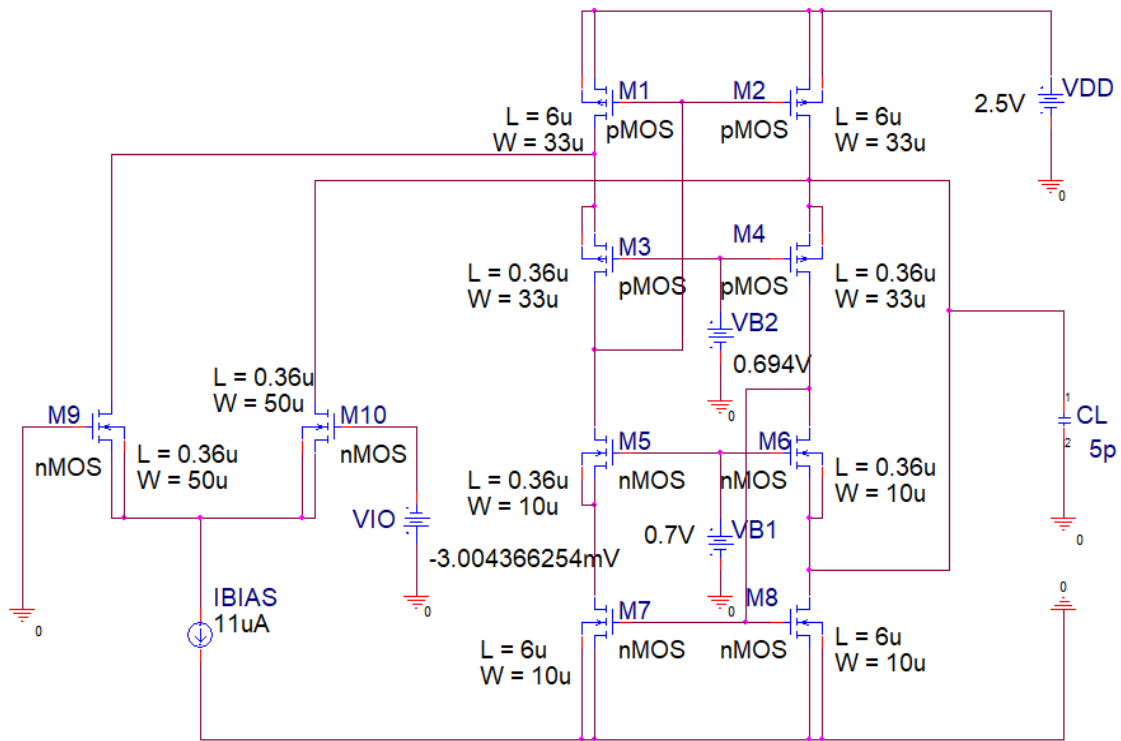


Figure 4.1: Design of Single-Ended Output Folded Cascode CMOS Op-Amp.

4.2 Simulation and Data Analysis

4.2.1 DC Analysis

DC analysis calculates the state of a circuit with steady (non-time varying) inputs after a period of time. It includes bias point analysis and DC sweep analysis.

Bias point analysis

The bias point analysis is used to measure the operating points of the design circuit.

Like node voltages, node currents, and power dissipation.

A) Node voltages

Ideally, when both inputs of the op amp are grounded (0V), the output offset voltage is zero. But practically this is not true. For the op amp designer, one main task is to check whether the output offset voltage is zero or nearly zero when both inputs are zero. If it is not zero, the op amp designer must make sure that the output offset voltage is zero or close to zero by applying some input offset voltage. In our initial design, when both inputs were grounded (0V), we have found that, the output offset voltage was not zero. But, by iterative trial and error method, we were able to reduce the output offset voltage to 80.53pV by applying a very small input offset voltage of -3.004368254mV to the noninverting input terminal. The node voltages and the output offset voltage obtained from PSPICE simulations are shown in figure 4.2.

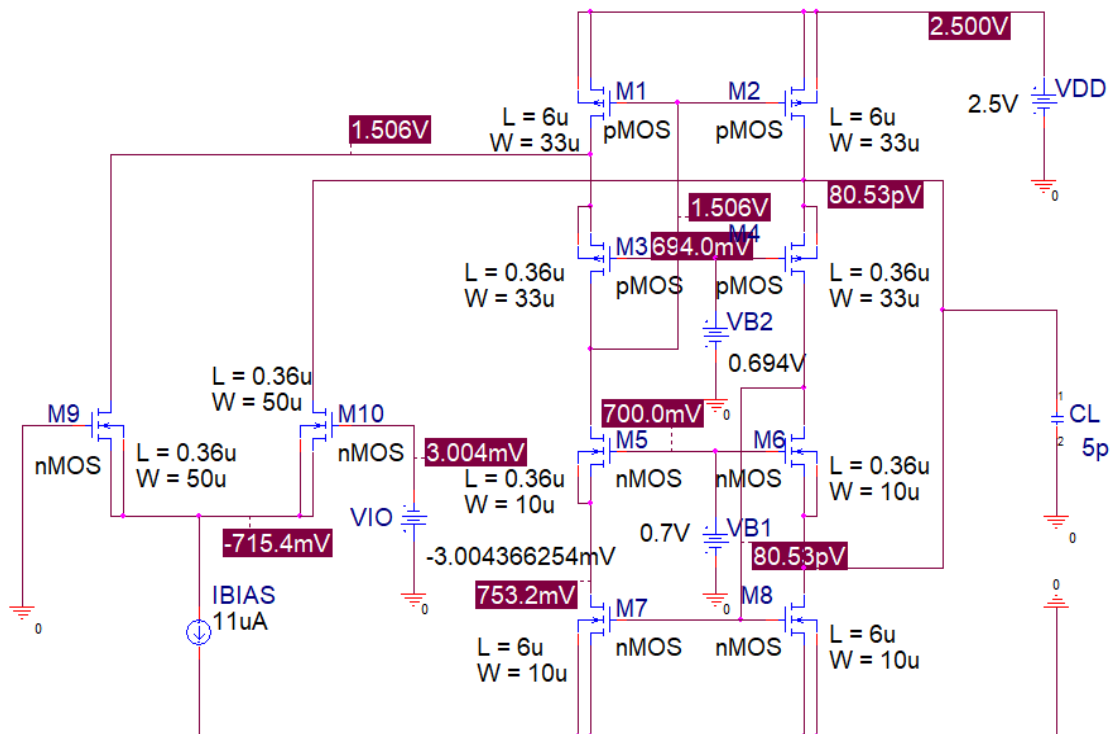


Figure 4.2: Simulation Results of Node Voltages.

C) Power Dissipation:

Figure 4.4 is the simulation result of the power dissipation of the circuit.

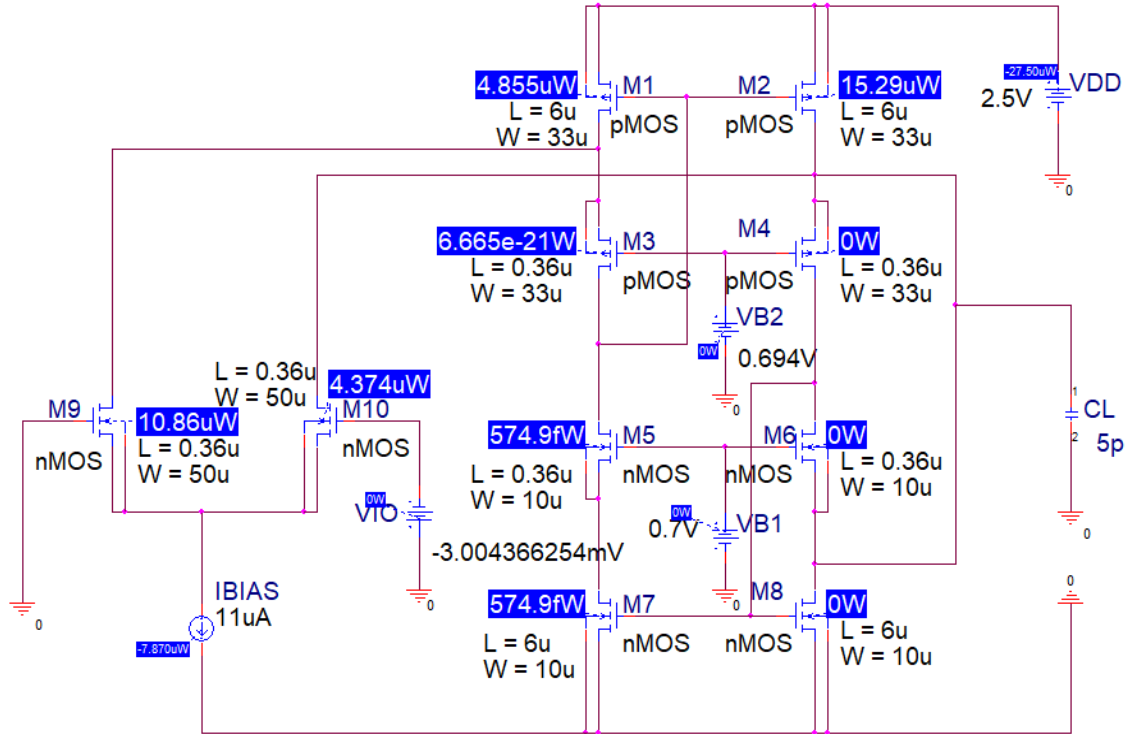


Figure 4.4: Simulation Results of power dissipation.

The total power dissipation is calculated as follows:

$$P_D = (10.86 + 4.374 + 4.855 + 15.29)\mu_W + (6.665 \times 10^{-6} + 574.9 + 574.9)fW \quad (4.2.1)$$

$$\Rightarrow P_D = (10.86 + 4.374 + 4.855 + 15.29)\mu_W + (0.000006665 + 1,149.8) \times 10^{-15}W$$

$$\Rightarrow P_D = (35.379)\mu_W + (1.149800006665) \times 10^{-12}W$$

$$\Rightarrow P_D = 35.379001149800006665\mu_W = 0.035379mW \quad (4.2.2)$$

Thus, the total power consumed by the device is 0.035379mW. This shows that, the power consumed by the device is too small. Therefore, this device can operate for longer duration of time and applied for portable and hand-held devices.

DC Sweep; ICMR

The DC analysis is used to calculate the state of circuit elements with fixed (time independent) input(s) after an infinite period of time, i.e. DC sweeps steadily the state of voltage, current and other digital systems when sweeping as source model parameter over a range of value. It is the mechanism of simulating ICMR. The input common mode range (ICMR) is the range of voltage for which the input differential pair will remain in saturation. This range is determined by the amplifier structure, transistor sizes, and bias currents. The circuit design to simulate the ICMR is shown in figure 4.5. For linearity test, the single-ended output folded cascode CMOS op amp is biased in the unity gain (voltage follower) configuration.

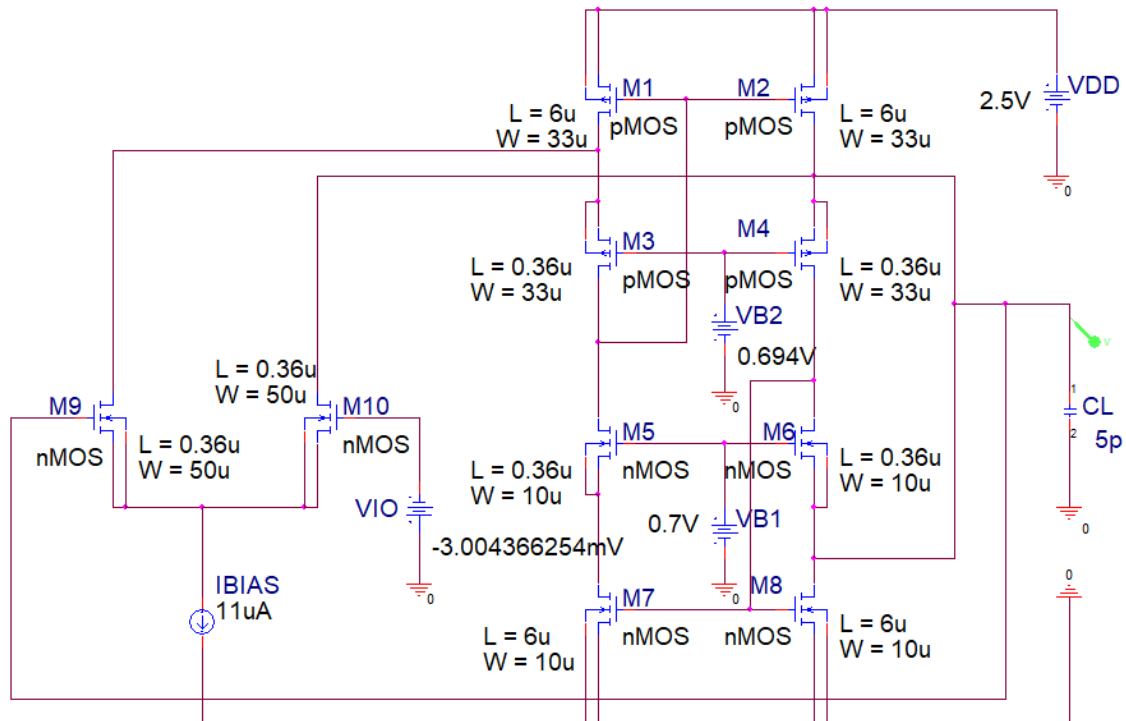


Figure 4.5: Circuit Design for the ICMR Analysis.

From the simulation result shown in figure 4.6, we observe that the graph is linear for input voltage ranging from -536.000mV to 1.0066V .

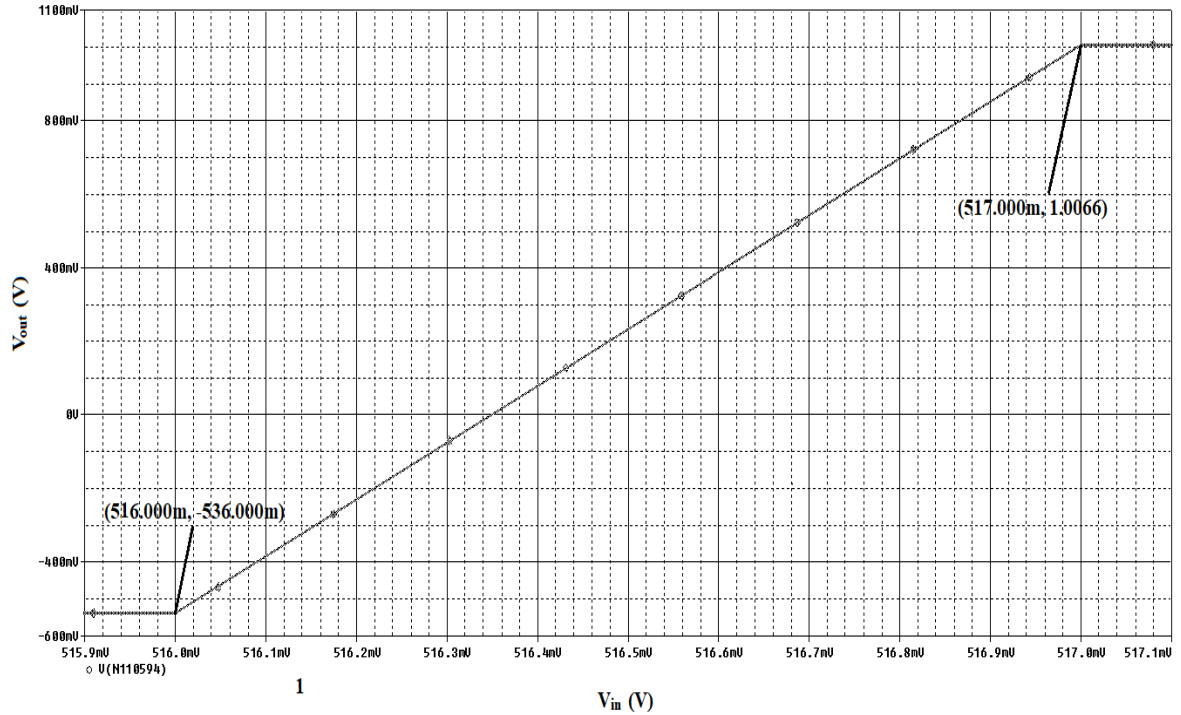


Figure 4.6: Simulation Result of ICMR.

4.3 AC Analysis

AC sources are time dependent and the circuit has input small signals as a function of frequency applied to both the input terminals. The output value of the AC signal varies over a range of frequencies in phase or out of phase with respect to the input values of the AC signal and it also depends on the sign of the input AC signal. AC analysis consists of AC sweep/noise (DC open loop gain and CMRR) and Transient/time domain analysis (output voltage swing and SR).

A) AC Sweep/Noise Analysis: Open Loop Gain, GBW and PM

The open loop gain was measured using the circuit design shown in figure 4.7. In this configuration, the amplifier is an open loop mode with 2.5V supply voltage. An

AC signal of 1V is applied at the gate of M_9 and a DC input offset voltage of -3.004366254mV is applied to the gate of M_{10} .

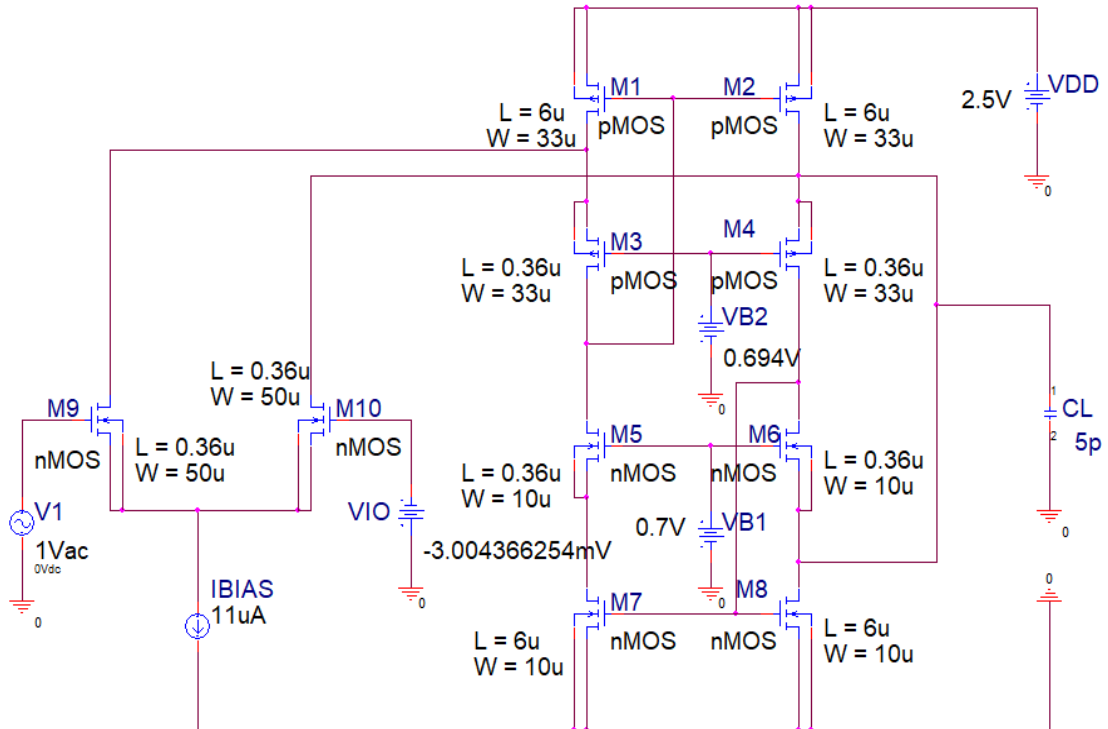


Figure 4.7: Circuit Design of Open Loop Gain and PM.

The simulation results of the open loop gain, GBW, and PM are shown in figure 4.8. From the simulation results, we have achieved the following values:

- The open loop gain is found to be 54.013dB
- The -3dB cut-off frequency is 44.996KHz ; we have achieved a very wide unity gain frequency of 14.03MHz respectively,
- The phase difference is 0° and phase margin is 67.337° .

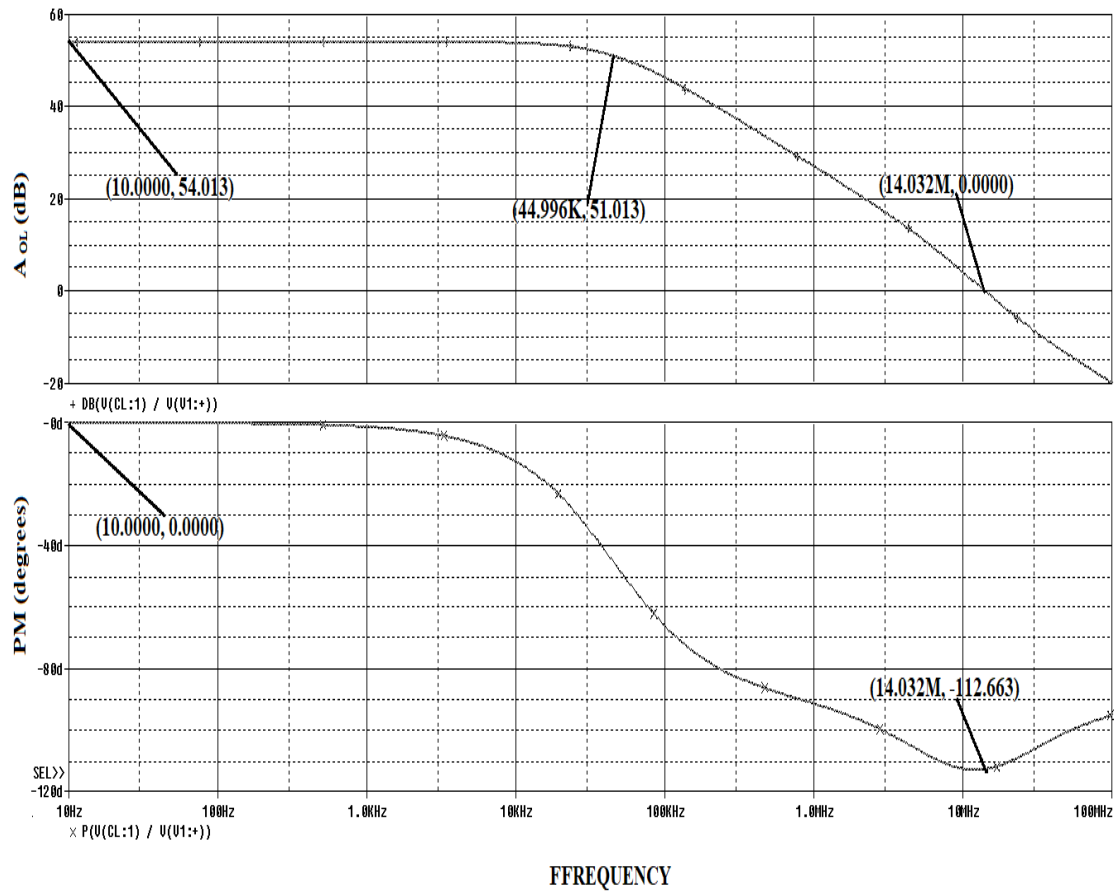


Figure 4.8: Simulation Result of Open Loop Gain, GBW, and PM.

CMRR:

The circuit design to measure the CMRR is shown in figure 4.9. In this configuration a 1V AC input signal and a -3.00436625 mV DC voltage are connected common to both the inverting as well as the non-inverting terminals.

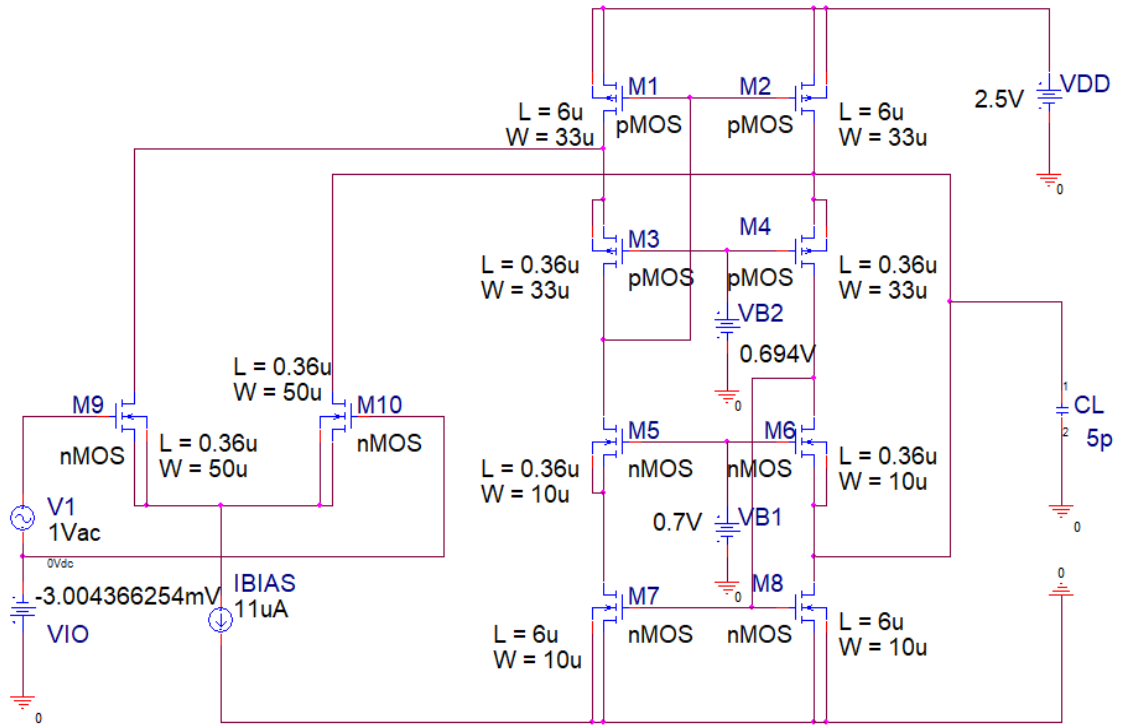


Figure 4.9: Circuit Design for CMRR Analysis.

The simulation result of the CMRR is shown in figure 4.10, in which $\text{CMRR} = 52.138\text{dB}$.

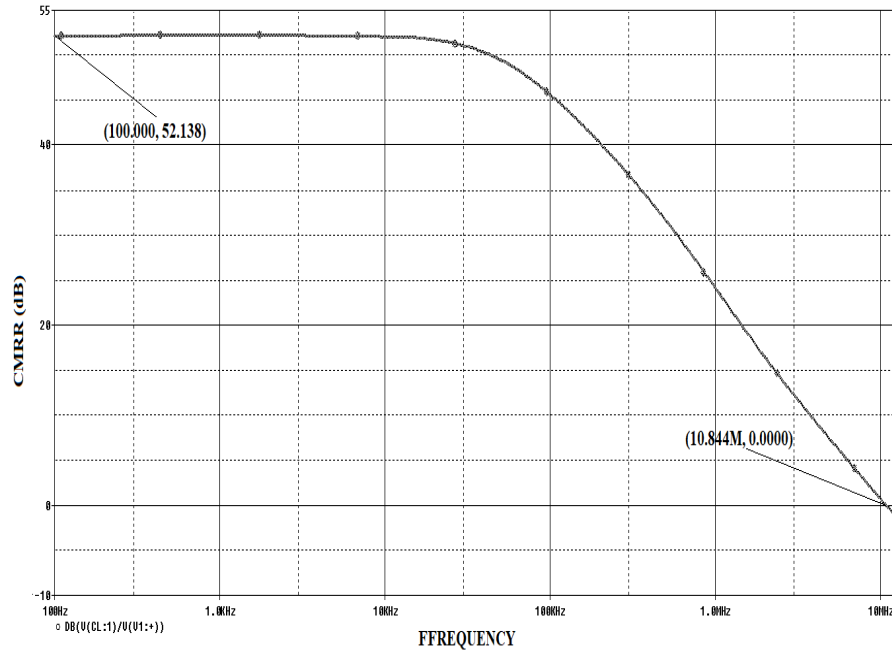


Figure 4.10: Simulation Result of CMRR.

B) Transient (Time Domain) Analysis:

Transient (time domain) analysis is probably the most popular analysis. The output AC signal tries to follow the input signal with out distortion or clipping for some amplitudes of the input AC signal.

Input and Output Voltage Swings:

The circuit design to measure the input and output voltage swings is shown in figure 4.11. A sinusoidal voltage of $750 \mu V$ amplitude with frequency 100Hz is connected to the inverting terminal and a DC input offset voltage of $-3.004366254 mV$ is applied to the noninverting terminal.

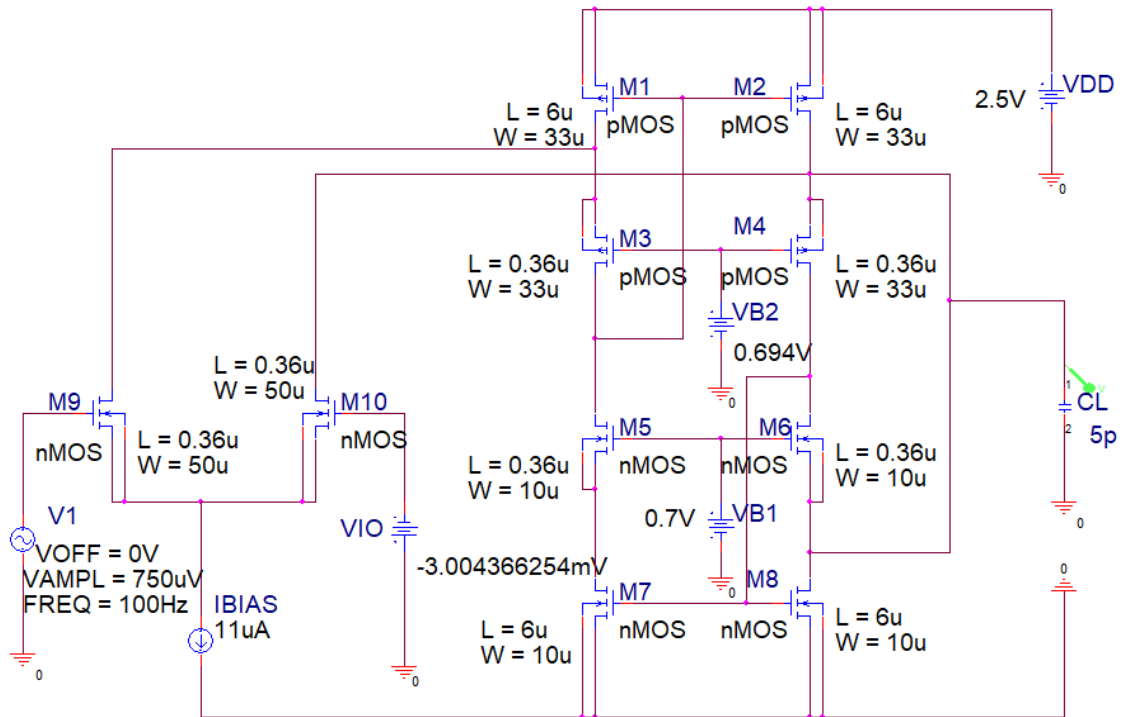


Figure 4.11: Circuit Design to Measure the Voltage Swing.

Figure 4.12 shows the simulation results of the input and output voltage swings. When an input peak-to-peak signal of 1.52mV is applied, the output sinusoidal voltage is found to be amplified, that is, the peak-to-peak output signal is 1.5mV.

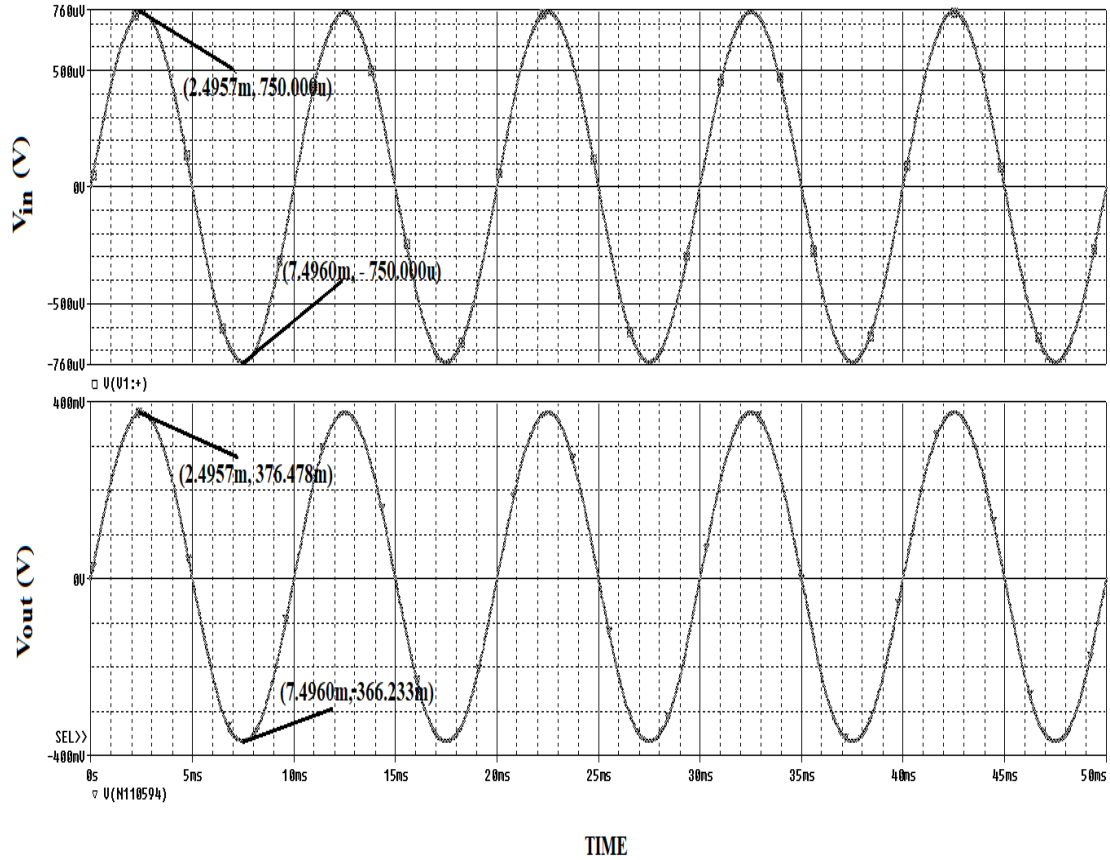


Figure 4.12: Simulation Result of Voltage Swing.

The voltage gain (A) is calculated as follows:

$$A = \frac{V_{out}}{V_{in}} = \frac{376.478mV - (-366.233mV)}{1.5mV} \quad (4.3.1)$$

$$\Rightarrow A = \frac{740.711mV}{1.5mV} = 493.80733$$

$$\Rightarrow A = 20 \times \log(493.80733) = 20 \times 2.69355753 = 53.8712dB \quad (4.3.2)$$

Also, the output voltage and the input voltage are in phase (0°). Thus, these results are in agreement with the simulation results obtained from the AC sweep/noise analysis for open loop DC gain and the phase difference.

In figure 4.13, to measure the slew rate, a step input signal (i.e., a square wave, VPulse) of 5V peak-to-peak voltage and 1ms period is applied at the noninverting terminal, while the inverting terminal is connected to the output terminal (unity gain configuration). The slew rate is determined from the slope of the rising and the falling edges of the output wave.

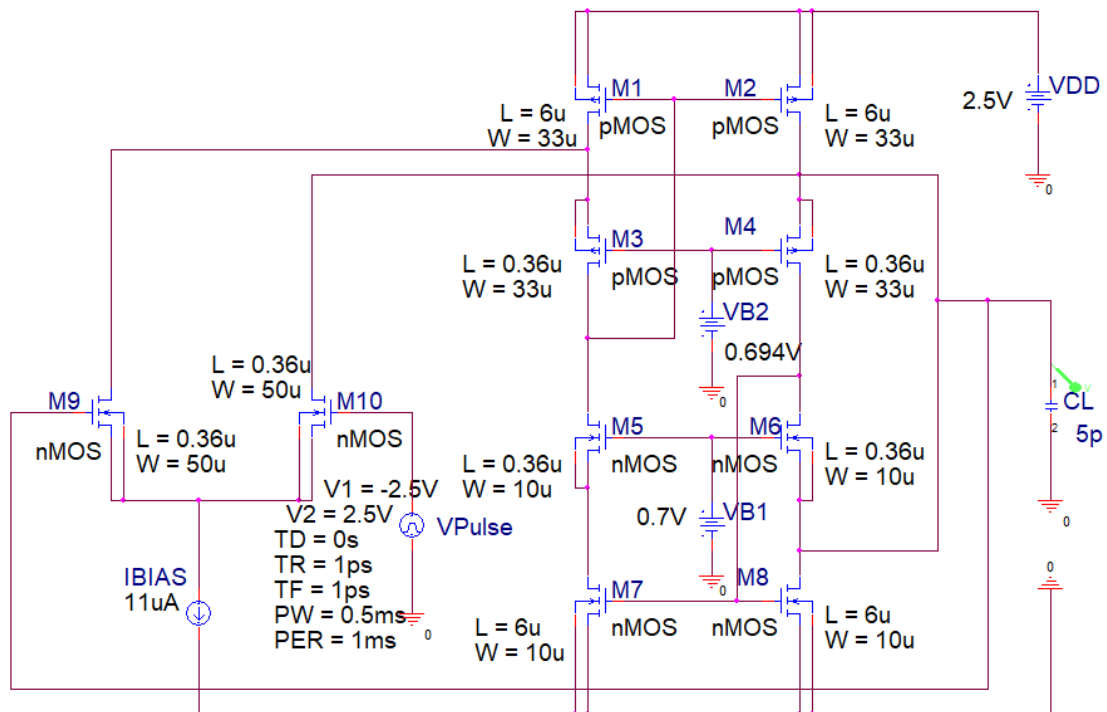


Figure 4.13: Circuit Design for SR Analysis.

The slew rate simulation result is shown in figure 4.14. The slew rate for the rising

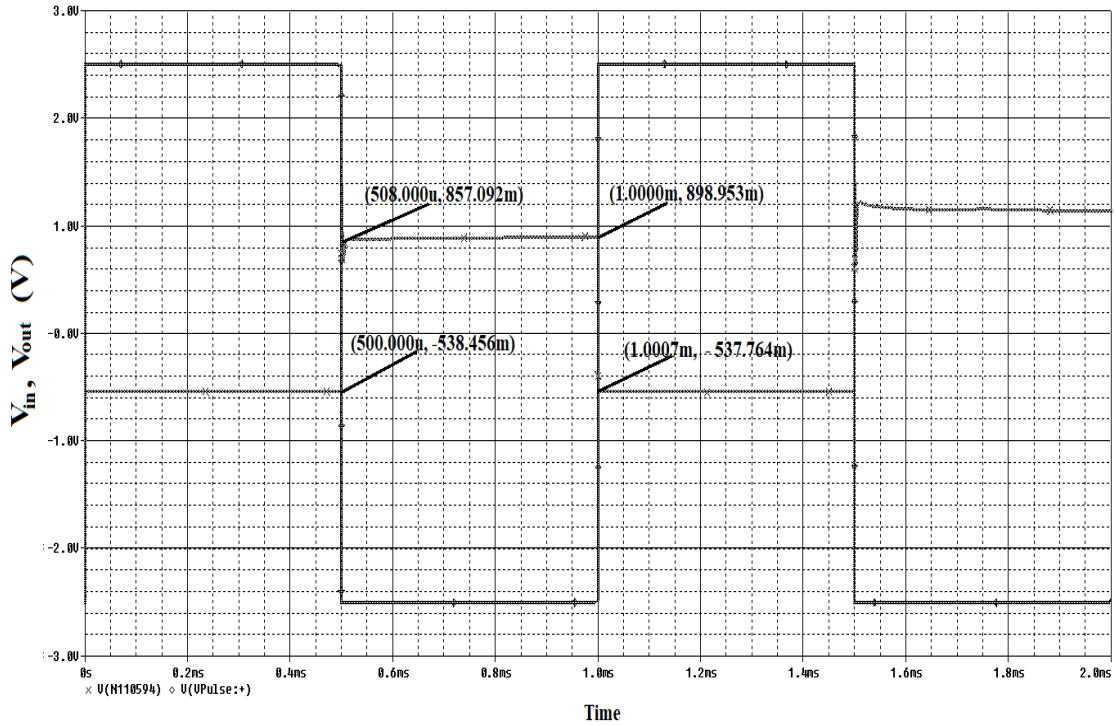


Figure 4.14: Simulation Result of SR.

edge (SR_+) was found to be:

$$SR_+ = \frac{857.092mV - (-538.456mV)}{508.000\mu s - 500.000\mu s} \quad (4.3.3)$$

$$SR_+ = \frac{1,395.548mV}{8\mu s} = \frac{1.395548V}{8\mu s} = 0.17V/\mu s$$

The slew rate for the falling edge (SR_-) was found to be:

$$\Rightarrow SR_- = \frac{-537.764mV - 859.953mV}{1.0007ms - 1.0000ms} \quad (4.3.4)$$

$$\Rightarrow SR_- = -1.9967V/\mu s = -2.00V/\mu s$$

Therefore, we observe that the positive slew rate (SR_+) = 0.17 V/ μ s and the negative slew rate (SR_-) = -2.00 V/ μ s.

Table 4.1: Comparison Between Proposed Value with Simulation Result

S.NO	Parameter	Proposed value	Simulation result
1	P_{diss}	$5mW$	0.035379mW
2	ICMR	$-2.4V$ to $2.4V$	$-536.000mV$ to $1.0066V$
3	CMRR	$50dB$	52.138dB
4	Gain	$\geq 50dB$	54.013dB
5	GBW	$\geq 9.8MHz$	14.03MHz
6	SR	$6V/\mu_s$	$0.17V/\mu_s$; $-2.00V/\mu_s$
7	PM	$\geq 45^\circ$	67.336°

Chapter 5

CONCLUSIONS AND RECOMMENDATIONS

5.1 Conclusion

The design and simulation results were analyzed for the optimum performance of the proposed single-ended folded cascode CMOS op-amp circuit to achieve the research objectives. It has been challenging to match hand calculation with simulation results. As a result, after the simulations, most of the transistors sizes were modified in order to optimize various performances. In fact, when designing a circuit, the hand calculations give scientific guess for all parameters, while simulation with PSPICE software shows the results closer to the real circuit performance values.

From our results of performance parameters, we can conclude that the single-ended output folded cascode CMOS op amp circuit design has negligibly low power dissipation (0.043mW) which is very important for hand-held devices such as mobile phones and other portable field instruments. The design has wide GBW (14.03MHz), moderate gain (54.013dB), moderate CMRR (52.138dB) and good ICMR (from -536.000mV to 1.0066V).

5.2 Recommendations

We have achieved a very good single-ended output folded cascode CMOS op amp. But, in the future the researcher will investigate the following parameters to improve the performance of the design: slew rate, ICMR, Open loop gain and PSRR.

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Declaration

I, hereby declare that the thesis is my original work and has not been presented for a degree in any other university, and that all sources of materials have been dully acknowledged.

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